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Safe Operating ARea for power transistors

T. W. GATES and M. F. BALLARD

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A method of graphically presenting the Safe Operating ARea for power transistors has been established and the name of this area has been abbreviated to SOAR.

This article explains how the forward-bias SOAR curves published in Mullard data have been constructed paying particular attention to the method used in the Mullard Quality Laboratory for measuring and fixing the second breakdown boundary. It further explains how the published d.c. SOAR limits have been extended for repetitive square-wave pulse operation. A simple method is then given for using the published SOAR data for most applications. This method is expanded to cover practical waveforms of a non-repetitive and non-square nature. Brief reference is also made to reverse-bias second breakdown protection.

Examples using power transistors in audio, switching, and r.f. applications are included.

INTRODUCTION

One of the main restrictions in the operation of power transistors is the phenomenon known as 'second breakdown'. This is the name given to a transistor condition whereby the collector-emitter voltage abruptly switches from a high to a low voltage value with increased current. Second breakdown is normally destructive and straightforward rules for avoiding this condition have been formulated and are presented on page 51. In this section a brief account of second breakdown is given while a more detailed description is presented later in the text.

A diagram illustrating the output characteristics of a power transistor is shown in Fig. 1. It is not representative of any particular device but merely serves to demonstrate the I_C against V_{CE} characteristics of a transistor as it goes into second breakdown. On the horizontal axis the forward and reverse-biased base regions are clearly grouped, with the base open-circuit condition dividing the two regions.

The transistor will enter second breakdown at a certain critical current value which is low at high collector-emitter voltages and higher at low voltages. Three loci for critical current values are shown on the diagram; these represent d.c., pulse, and short pulse operation. The extension of the second-breakdown locus for pulse operation is dependent on the pulse duration t_p and also, to a lesser extent, on the duty cycle d (see Fig. 8). Thus the greatest extension is permissible with single-shot pulses (d=0·01) of short duration, say 10μs. (The value d=0·01 can be considered as single-shot because there is ample time for cooling between power pulses.)

Observation of second breakdown

Consider the I_C against V_{CE} characteristic ABCDE shown in Fig. 1. At point B the device goes into avalanche, otherwise known as first breakdown. At this point the collector current starts to rise sharply for very little increase in the collector-emitter voltage. If the current is allowed to increase up to a critical value at C the device will enter second breakdown. This is noted by an abrupt switching of the collector-emitter voltage to a low value at point D. In second breakdown the device offers only a very low resistance to collector current, and is invariably destroyed if the current is not specially limited by a circuit external to the transistor. Beyond point C the process is generally irreversible whereas up to point C in avalanche the trace can be returned with no serious alteration to the transistor properties. It is in the forward-biased mode of operation that the phenomenon of second breakdown has been extensively studied over recent years, and a method of presenting the Safe Operating ARea (abbreviated to SOAR) is now being published in Mullard data for power transistors.

In many applications, however, the reverse-bias breakdown characteristics are also of importance. For example, when a power transistor with an inductive load is turned off by reverse biasing the base, the collector voltage will rise above the supply voltage because of the stored inductive energy of the coil. For such applications transistors have been developed which permit excursions outside the V_{CEO}max rating under specified conditions. This is discussed later.

With reverse bias on the base, second breakdown is always preceded by first-breakdown. At low collector currents the voltage across the transistor can exceed the V_{CEO} rating as shown in Fig. 1. In first breakdown, or avalanche, the device goes through a negative resistance region until a critical current value is reached at which point the collector-emitter voltage abruptly switches to a very low value in second breakdown.

Fig. 2 shows a photograph of the avalanche characteristics of a power transistor and Fig. 3 depicts an actual second breakdown. The moment of switching of the

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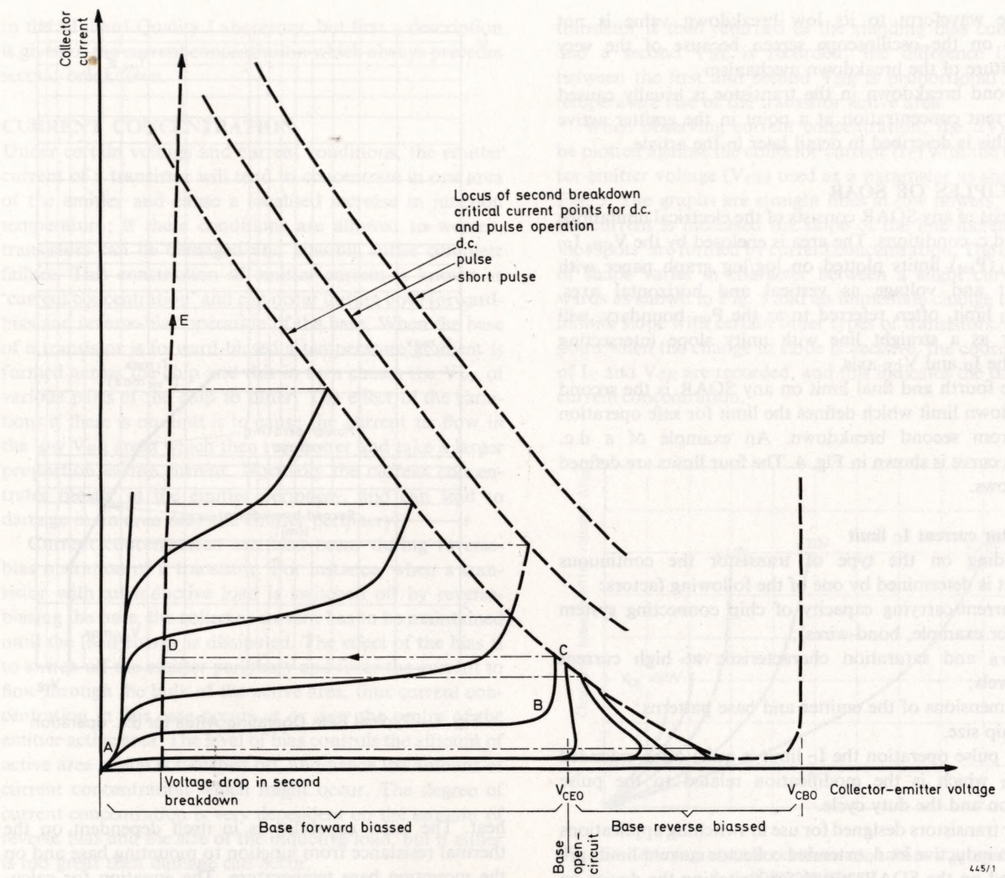

Fig. 1—Output characteristics of a power transistor

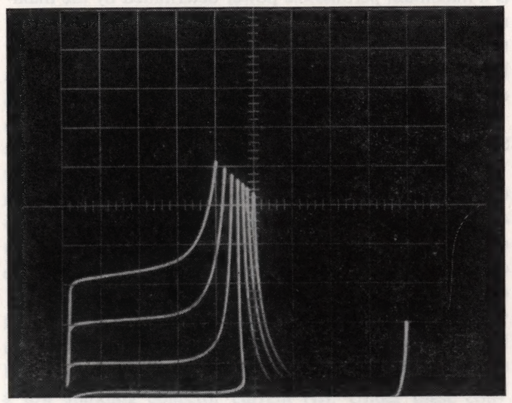

Fig. 2—Oscillogram of avalanche in a typical power transistor

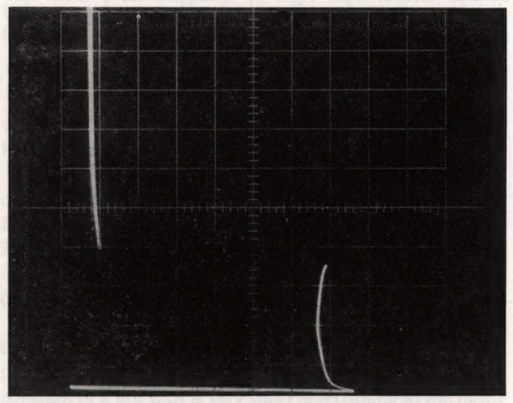

Fig. 3—Oscillogram of second breakdown in a typical power transistor

voltage waveform to its low breakdown value is not visible on the oscilloscope screen because of the very fast nature of the breakdown mechanism.

Second breakdown in the transistor is usually caused by current concentration at a point in the emitter active area; this is described in detail later in the article.

PRINCIPLES OF SOAR

The basis of any SOAR consists of the electrical limitations under d.c. conditions. The area is enclosed by the V_{CE}, I_C, and T_j (P_{tot}) limits plotted on log/log graph paper with current and voltage as vertical and horizontal axes. The T_j limit, often referred to as the P_{tot} boundary, will appear as a straight line with unity slope intersecting both the I_C and V_{CE} axis.

The fourth and final limit on any SOAR is the second breakdown limit which defines the limit for safe operation free from second breakdown. An example of a d.c. SOAR curve is shown in Fig. 4. The four limits are defined as follows.

Collector current I_C limit

Depending on the type of transistor the continuous I_C limit is determined by one of the following factors:

1) current-carrying capacity of chip connecting system (for example, bond-wires);
2) h_{FE} and saturation characteristic at high current levels;
3) dimensions of the emitter and base patterns;
4) chip size.

Under pulse operation the I_C limit is quite often extended to I_{CM} which is the modification related to the pulse duration and the duty cycle.

For transistors designed for use in switching applications with an inductive load, extended collector current limits are specified on the SOAR curves for switching the device on and off under specified time conditions (for example, see the data on the BDY93 transistor). Transistors specifically designed for switching off the current in highly inductive loads such as relays, may have a collector current limit specified as a function of load inductance with the base reverse biased. This class of transistor have their safe operating region specified in terms of load inductance or load energy, as in the data for the BSW66 series.

Collector-emitter voltage V_{CEO} limit

The V_{CEO} limit is the maximum permissible collector-emitter voltage for all forward-biased base conditions; even under pulse conditions this limit must not be exceeded because breakdown would then be extremely probable.

With some devices the level of the V_{CEO} limit can be exceeded in reverse-biased base operation provided the time and low-current conditions stated in the data are observed. In these cases, reverse-bias (or zero bias) ratings are used, such as V_{CEX} and V_{CER} if a resistive path is provided between emitter and base.

Power dissipation P_{tot} limit

The permissible steady state power dissipation in a transistor depends both on its maximum permissible junction temperature and on the ability of the device to dissipate heat. The latter capability is in itself dependent on the thermal resistance from junction to mounting base and on the mounting base temperature. The equation for calculating the maximum permissible power dissipation is:

$$P_{tot}max = \frac{T_jmax - T_{mb}}{R_{th}(j-mb)}, \qquad \ldots(1)$$

From Eq. 1 it can be seen that for any value of T_{mb} there is a maximum permissible power determined by the maximum junction temperature $T_j$max and the thermal resistance $R_{th}(j-mb)$. This power constraint is plotted on the logarithmic scale of the SOAR curve and appears as a line of unity slope joining the V_{CE} and I_C limits.

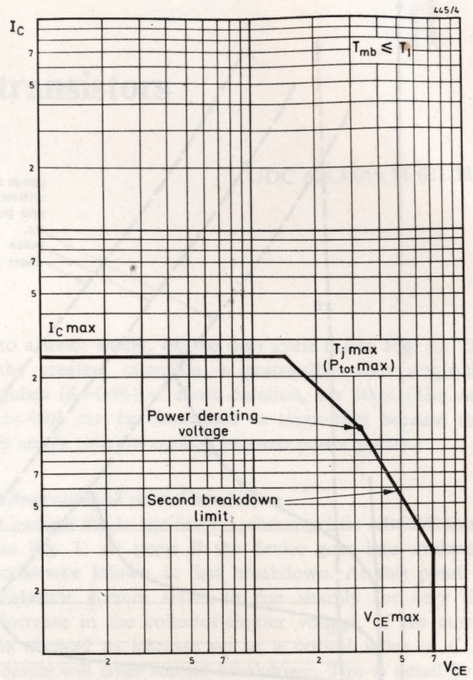

Fig. 4—Typical Safe Operating ARea for d.c. operation

Second breakdown limit

When a transistor is operating under maximum power (that is, along the P_{tot} limit), the uniformity of the current and therefore the temperature distribution over the active chip area changes as the voltage component V_{CE} is increased. The voltage above which this occurs is clearly seen on the typical d.c. SOAR curve shown in Fig. 4. This voltage is called the 'power derating voltage' because beyond this value, the only way to maintain the thermal stability is to derate the power. This leads to a fourth boundary where the maximum allowable power is reduced. This fourth and final line is the 'second breakdown limit' and completes the enclosure of the SOAR. The next few sections outline how this limit is measured and drawn

in the Mullard Quality Laboratory, but first a description is given of the current concentration which always precedes second breakdown.

CURRENT CONCENTRATION

Under certain voltage and current conditions, the emitter current of a transistor will tend to concentrate in one area of the emitter and cause a localised increase in junction temperature; if these conditions are allowed to worsen, transistors can be damaged and possibly suffer complete failure. This constriction of emitter current is known as 'current concentration' and can occur during both forward-bias and reverse-bias operation of the base. When the base of a transistor is forward-biased a temperature gradient is formed across the chip and this in turn causes the V_{BE} of various parts of the chip to differ. The effect of the variations if there is no limit is to cause the current to flow in the low V_{BE} areas which then run hotter and take a larger proportion of the current. Normally the current concentrates mostly in the emitter periphery, and can lead to damage in an area near the emitter periphery.

Current concentration can also occur during reverse-bias operation of a transistor. For instance, when a transistor with an inductive load is switched off by reverse-biasing the base, the collector current has to be maintained until the load energy is dissipated. The effect of the bias is to switch off the emitter periphery and force the current to flow through the bulk of the active area, thus current concentration in this case occurs at or near the centre of the emitter active area. The level of bias controls the amount of active area which is switched off, and hence the amount of current concentration which might occur. The degree of current concentration is very dependent on the amount of reverse bias and the size of the inductive load, but if either is too great then damage can occur.

Clearly, if a transistor is to give reliable service in either forward or reverse-bias operation the area of operation must be controlled in such a way that damage does not occur. The SOAR curves must therefore define an area that not only precludes second breakdown but also the current concentration that precedes it.

Detecting current concentration

When the emitter current contracts, it causes all the current and heat generated to be concentrated at one point on the emitter. Observations of the transistor chip with a thermal detector, such as an infrared microscope, will show this thermal asymmetry and therefore this method can be used to detect the onset of current concentration. Although the infrared method is very accurate and sensitive, it has the disadvantage of needing exposed chips for the observation to be made. Therefore, a method which can be used on encapsulated transistors is more desirable.

A suitable method for monitoring current concentration follows the usual technique for measuring the thermal resistance (R_{th}) of a transistor (see Ref. 1). The transistor is biased with a specified collector-emitter voltage (V_{CE}) and a low standing collector current (I_S). Under these conditions the base-emitter voltage (V_{BE}) is recorded, and the transistor is switched from this standing bias to the dissipation power until thermal equilibrium is reached. The transistor is then returned to the standing bias condition and a second V_{BE} is recorded; the difference (ΔV_{BE}) between the first and second V_{BE} is proportional to the temperature rise of the transistor active area.

When observing current concentration, the ΔV_{BE} can be plotted against the collector current (I_C) with the collector-emitter voltage (V_{CE}) used as a parameter as shown in Fig. 5. The graphs are straight lines at low powers, but as the current is increased the slope of the line increases as 'hot spots' are formed by current concentration. The change of shape varies in character between a slight curve upwards as shown in Fig. 5 and an immediate change to near infinite slope with certain other types of transistors. At the point when the change in slope is decisive, the coordinates of I_C and V_{CE} are recorded, and this indicates the onset of current concentration.

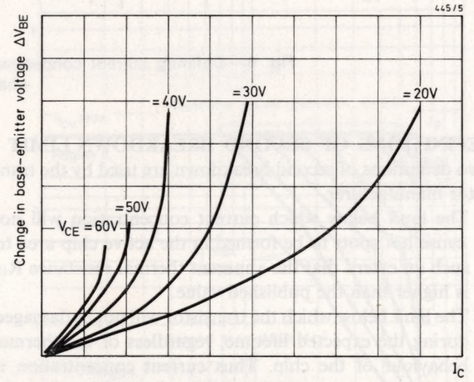

Fig. 5—Defining current concentration from V_{BE} against I_C characteristics

However, when a decisive change in slope is not evident, the onset of current concentration is not easily defined using the above method. In such cases, current concentration is determined by plotting the R_{th} against I_C characteristics as shown in Fig. 6 where R_{th} values are calculated from:

$$R_{th} = \frac{\Delta V_{BE}}{V_{CE} \times I_C \times S} \text{degC/W}, \qquad \ldots(2)$$

where S is the temperature coefficient of V_{BE} under the low standing current condition.

It will be observed from Fig. 6 that a basic value of R_{th} can be taken from the family of curves for R_{th} against I_C. In addition, the V_{CE} and I_C coordinates of the point where R_{th} has increased by a pre-determined amount are used to define the electrical conditions for the onset of current concentration.

In measuring the two V_{BE} values to calculate ΔV_{BE}, it is important to take the second V_{BE} measurement as soon as possible after the power is removed since the thermal time-constant of a hot spot is very short and cooling to the mean value of temperature is very rapid. If this precaution is not taken the device could enter current concentration before being detected.

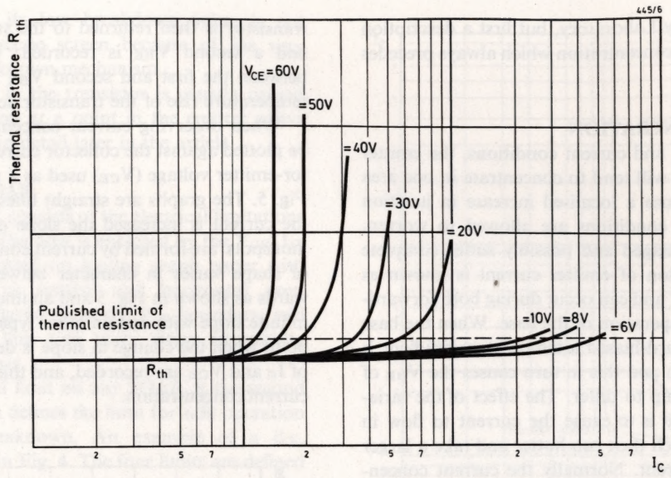

Fig. 6—Defining current concentration from thermal resistance R_{th} against I_C characteristics

DEFINITIONS OF SECOND BREAKDOWN LIMIT

Two definitions of second breakdown are used by the transistor manufacturer.

1) The limit below which current concentration will not cause hot spots to be formed in the active chip area to such an extent that the apparent thermal resistance R_{th} is higher than the published value.
2) The limit below which the transistor will not be damaged during the expected lifetime, regardless of the thermal behaviour of the chip. Thus current concentration is permitted, causing the R_{th} value to rise above the published value, provided second breakdown is not reached.

It can be seen that the first definition is more stringent and has a higher built-in safety factor than the second. Mullard use the first definition for most SOAR data, and the second is rarely used and only in special circumstances; that is, when it is necessary to allow for the possibility of an unusual circuit fault condition the first definition may be relaxed as defined under the second. However, where the second definition is applied, conclusive reliability evidence is always available before any such SOAR is published. A good example of an unusual fault condition referred to above is the overload seen by the audio power transistor when a stylus is scraped across a record, representing a totally abnormal (but nevertheless possible) condition in the application itself.

Forward and reverse-bias breakdown

The causes of second breakdown under forward and reverse-bias conditions are quite different. For this reason it is necessary to regard the two operational modes separately. It would be feasible to present two sets of SOAR information in published data; one to include a forward-bias second breakdown limit and the other to include a reverse-bias second breakdown limit. However, this is unnecessary because many applications do not require reverse-bias information in such detail. For this reason Mullard data places greater emphasis on SOAR curves for forward-bias operation.

Forward-bias second breakdown can be avoided by controlling the conditions applied to the transistor, but reverse-bias second breakdown is generally only avoidable by using some form of circuit protection such as a flywheel diode.

This article is concerned mainly with explaining the measuring, construction, and applications of the forward-bias SOAR. However, considerations for reverse-bias parameters are also discussed.

LABORATORY DERIVATION OF FORWARD-BIASED SOAR

SOAR for d.c. operation

The basis of all forward-biased curves shown in published data is the Safe Operating ARea under d.c. conditions. This area is defined by the four boundaries previously described with reference to Fig. 4, namely:

1) the maximum V_{CE} for forward-bias conditions;
2) the maximum I_C for d.c. conditions;
3) the thermal limit given by the limit R_{th} and $T_j$max, also known as the P_{tot} boundary;
4) the V_{CE} versus I_C line which is defined by current concentration, commonly called the second breakdown boundary.

The first three boundaries are easily measured and defined, but the fourth requires further explanation. The usual procedure, as carried out during quality assessment, for measuring the slope and position of the second breakdown boundary, is as follows:

1) with I_C at the maximum d.c. value, the V_{CE} is increased until current concentration occurs;
2) the current is reduced in convenient steps and the V_{CE} is increased and measured at each new point of current concentration;
3) this is continued until the maximum V_{CE} is reached.

The above measurements are repeated on sufficient transistors so that a second breakdown boundary can be drawn to accommodate even the worst-case transistor.

The four boundaries are then presented in a graphical form by plotting I_C against V_{CE} on a log/log scale, which gives an approximate straight line for the second breakdown boundary.

A d.c. SOAR curve is illustrated in Fig. 7. This shows an example of measured current concentration points and indicates the amount of safety tolerance included. The safety tolerance will depend on the scatter of the measured values and on the factory reliability assessment results, but is always made large enough to avoid failures.

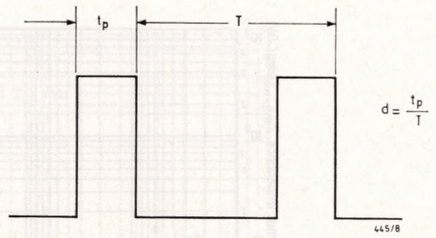

Fig. 8—Relationship between duty cycle (d), pulse duration (t_p) and period (T)

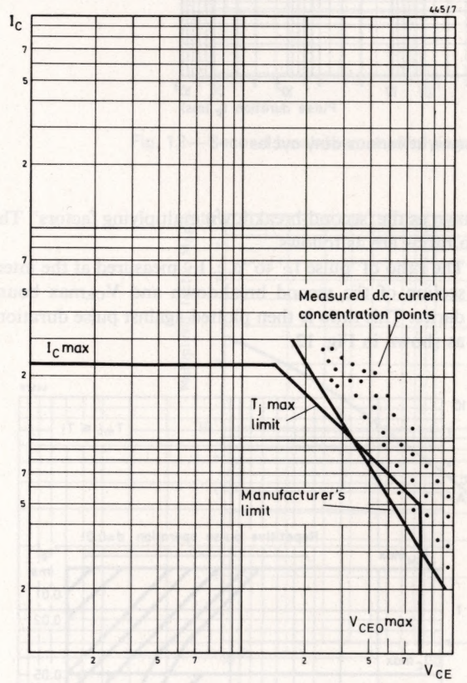

Fig. 7—Example of d.c. SOAR showing measured current concentration points

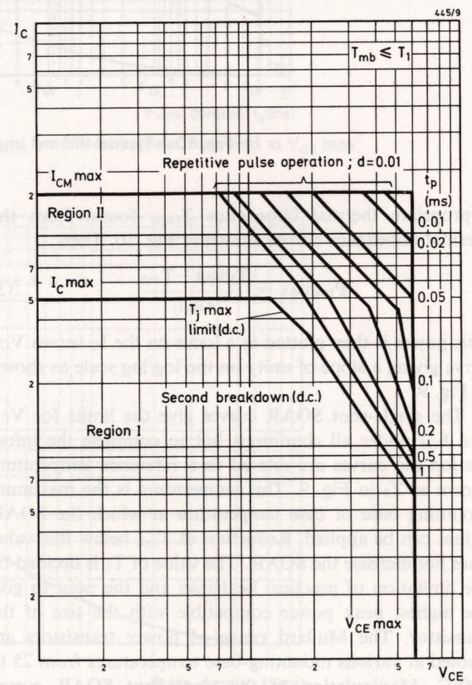

Fig. 9—Family of SOAR curves at duty cycle d = 0·01:
Region I shows permissible area for d.c. operation
Region II shows extended area for various values of t_p

SOAR family at 1% duty cycle

When a transistor is required to operate under pulse power the SOAR is extended beyond the d.c. area defined by the four boundaries described above. For any combination of pulse duration t_p and duty cycle d (defined in Fig. 8), the Safe Operating ARea could be measured using the same method as for d.c. SOAR. However, this is not practicable for the infinite number of conditions that could arise and so a method has been developed for calculating the SOAR for any pulse condition. This method uses as its basis a family of curves for pulse operation at a duty cycle of 1% (d = 0·01). From these curves, shown in Fig. 9, the SOAR for any specific duty cycle and pulse duration can be calculated. The pulse limits for the 1% duty cycle (d = 0·01) curves, often referred to as 'single-shot' curves, are measured and defined during quality assessment in a similar manner to that for the d.c. area.

The P_{tot} boundary for each pulse duration at 1% duty cycle is determined by specifying the maximum junction temperature ($T_j$max) and the mounting base temperature (T_{mb}) for which the rating applies. The maximum allowable power is then determined by dividing the difference between these two temperatures ($T_j$max−T_{mb}) by the

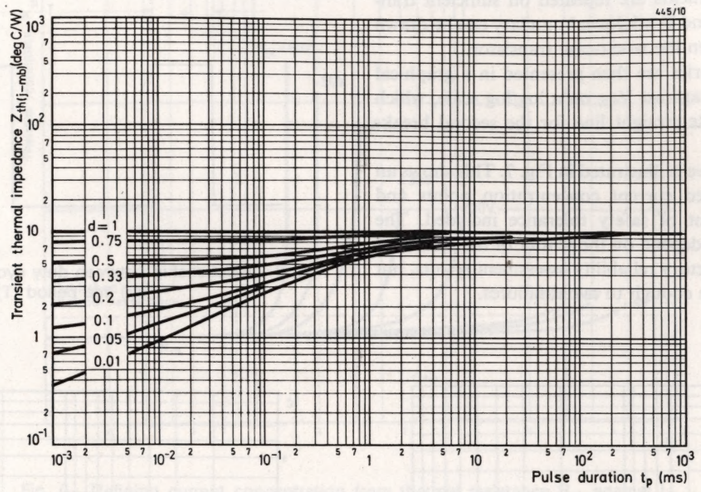

Fig. 10—Typical thermal impedance curves at various duty cycles

appropriate thermal impedance $Z_{th(t)}$ found from the thermal impedance curves shown in Fig. 10. Then:

$$P_{tot}max = \frac{T_j max - T_{mb}}{Z_{th(t)}}. \quad \ldots(3)$$

This power is then plotted as a locus on the I_C versus V_{CE} curve giving a slope of unity on the log/log scale as shown in Fig. 9.

The single-shot SOAR curves give the limits for V_{CE} and I_{CM} under all conditions but to complete the information the curves are related to a reference temperature shown as T_1 in Fig. 9. This temperature is the maximum mounting base or case temperature at which the SOAR values can be applied. Reduction of T_{mb} below this value does not increase the SOAR. The value of T_1 is decided by the limitation of practical heatsinks and the need to give the highest peak power compatible with the size of the transistor. The Mullard range of power transistors are quoted at various mounting-base temperatures from 25 to 100°C. Manipulation of the single-shot SOAR curves shown in Fig. 9 can give a further family of curves at any specified duty cycle, but the same mounting-base temperature will apply.

The inclusion of a maximum temperature T_1 raises the question: what effect will temperature have on current concentration? Observations on the effects of increasing the temperature have shown that, at the point of current concentration, there is a slight reduction in V_{CE} at a fixed I_C value. This reduction is small enough to be protected by the normal publication safety tolerances and hence second breakdown can be considered as being independent of temperature for the purposes of all normal circuit design calculations.

Manipulation of 1% duty cycle curves

The method of calculating a specific SOAR involves measuring from the single-shot curves (Fig. 11) two ratios known as the 'second-breakdown multiplying factors'. The two ratios are as follows.

1) The ratio of 'pulse I_C' to 'd.c. I_C' measured at the intersection of the second breakdown and V_{CE}max boundaries. This ratio is then plotted against pulse duration, as shown in Fig. 12.

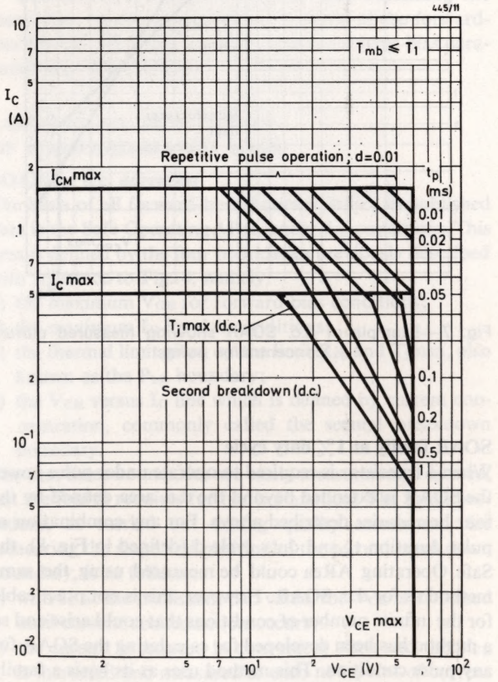

Fig. 11—SOAR family at 1% duty cycle: these curves are used to calculate breakdown multiplying factors

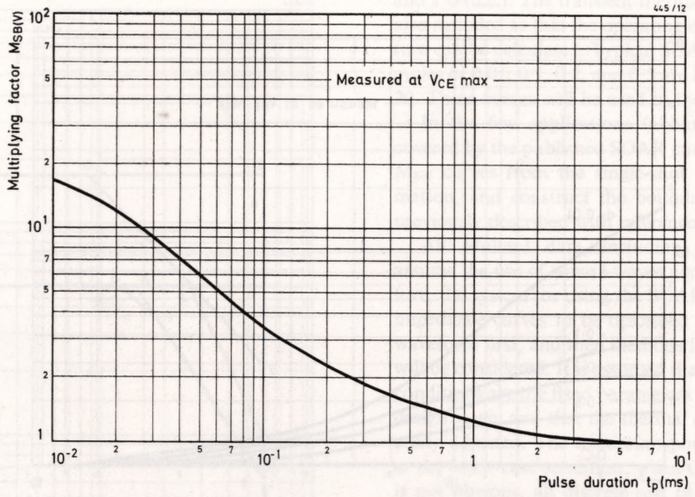

Fig. 12—Second breakdown multiplying factors $M_{SB(V)}$ for 1% duty cycle measured at V_{CE} max

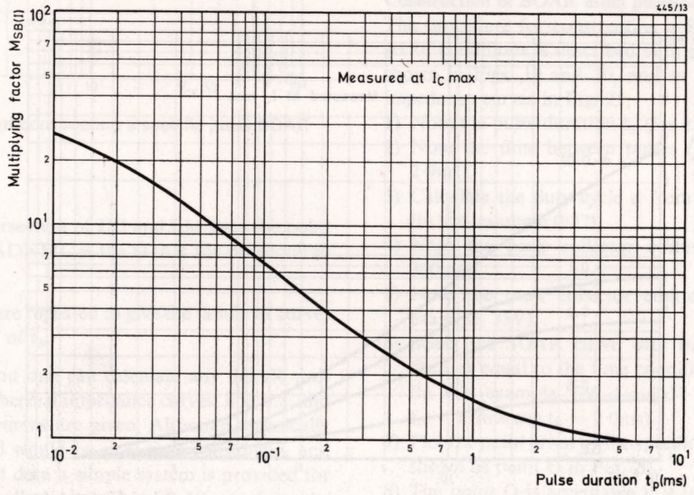

Fig. 13—Second breakdown multiplying factors $M_{SB(I)}$ for 1% duty cycle measured at I_C max

2) The ratio of 'pulse V_{CE}' to 'd.c. V_{CE}' measured at the intersection of the $I_C$max and the second-breakdown boundaries. The point is found by extending the second-breakdown limit until it cuts the $I_C$max line as shown in Fig. 11. This ratio is also plotted against pulse duration, as shown in Fig. 13.

The ratio determined at the V_{CE}max boundary is known as the second-breakdown multiplying factor at the V_{CE}max limit ($M_{SB(V)}$) and the other ratio is known as the second-breakdown multiplying factor $M_{SB(I)}$ at the $I_C$max limit.

These factors can then be used to determine second-breakdown boundaries for any pulse duration, but further manipulation is required to cover the effect of different duty cycles (d). Curves of multiplying factors at different duty cycles can be determined by using the following equation:

$$\frac{1}{M_{SB}} = d + \frac{1-d}{M_{SB(T+tp)}} + \frac{1}{M_{SB(tp)}} - \frac{1}{M_{SB(T)}}, \quad \ldots(4)$$

where:

M_{SB} = required multiplying factor for duty cycle (d) at pulse duration (t_p),

$M_{SB(T)}$ = multiplying factor for pulse duration T at d = 0·01,

$M_{SB(tp)}$ = multiplying factor for pulse duration t_p at d = 0·01,

$M_{SB(T+tp)}$ = multiplying factor for pulse duration ($T+t_p$) at d = 0·01.

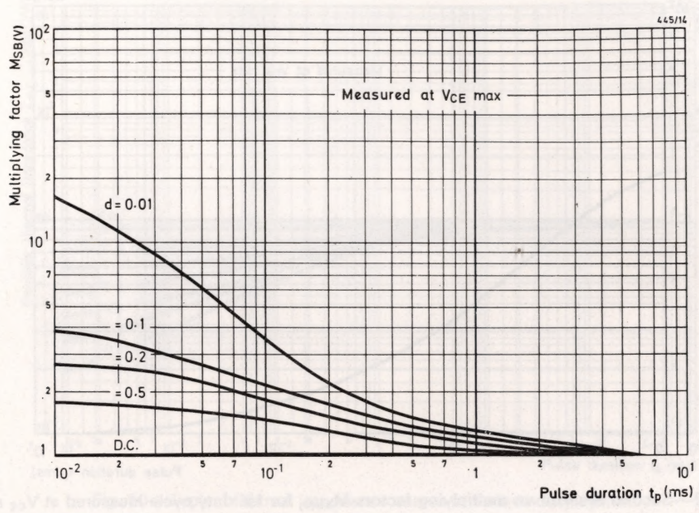

Fig. 14—Family of $M_{SB(V)}$ curves

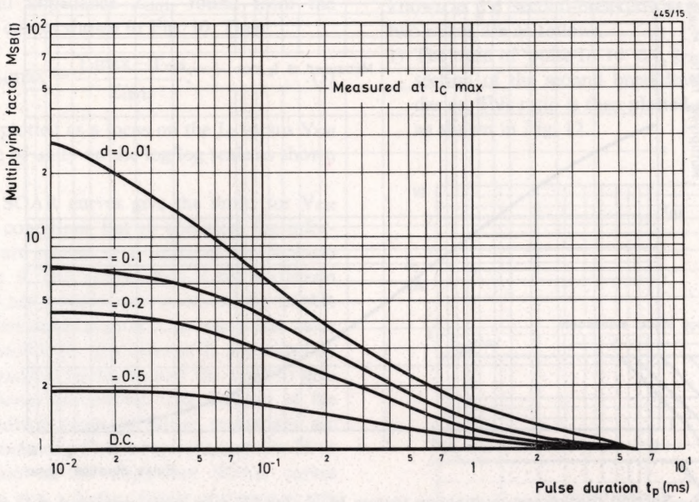

Fig. 15—Family of $M_{SB(I)}$ curves

This equation can be used to calculate both $M_{SB(V)}$ and $M_{SB(I)}$ values. Typical families of M_{SB} curves are illustrated in Fig. 14 for $M_{SB(V)}$ and Fig. 15 for $M_{SB(I)}$.

Construction of SOAR for specific pulse conditions using M_{SB} factors

The multiplying factors thus obtained can be used to calculate a family of SOAR curves having a fixed duty cycle as a fixed parameter and pulse duration as a variable parameter. The manipulation for determining a SOAR with a duty cycle (x) and pulse duration (y) is as follows.

1) The I_{CM} and V_{CE} boundaries for the particular application are drawn on log/log graph paper (lines AB and BC on Fig. 16).
2) The P_{tot} limit DE is constructed; this is achieved by determining the thermal impedance for the time condition (Fig. 10) and applying Eq. 3; that is:

$$P = \frac{T_{jmax} - T_{mb}}{Z_{th(t)}}.$$

3) The d.c. SOAR (FGHJC) is added to the graph, and the second breakdown boundary is extended to the I_C boundary at point K.
4) The multiplying factors for the required time condition at $t_p = y$ are calculated by the method previously described. The V_{CE} value at K is multiplied by $M_{SB(I)}$ to give L, and the I_C at J is multiplied by $M_{SB(V)}$ to give M.

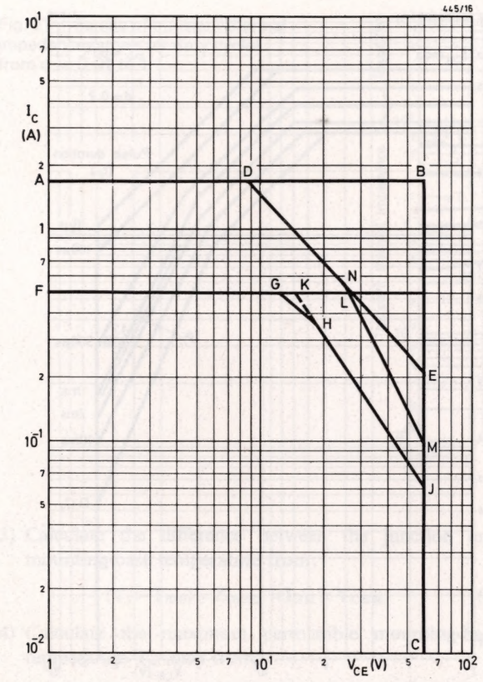

Fig. 16—Method of constructing a specific pulse SOAR

5) The point of intersection of DE and LM fixes the point N and the area ADNMC is the SOAR for the required time condition.
6) Points (1) to (5) are repeated to give the family of curves at various values of t_p.

Using this method one can calculate any SOAR provided the transient thermal impedance curves, and d.c. and single-shot SOAR curves are given. Although technically correct, this method would be very time consuming, and therefore in Mullard data a simple system is provided for the majority of applications: This is described in the following section.

SIMPLE METHOD OF USING PUBLISHED SOAR CURVES

The method previously described is being presented in a modified and simpler form in published data on power transistors. For each transistor sufficient SOAR information will be provided to cover 90% of all applications. Thus, in most cases the user will merely select the appropriate SOAR curve already constructed—without having to calculate and manipulate M_{SB} values.

In general, the data provides SOAR curves for pulse durations in multiples of 1, 2, 5, and 10, starting at pulse durations in the region 10 to 50μs. The families of curves are plotted at duty cycles of 0·01 (single-shot) 0·1, 0·2, 0·5, and 1·0 (d.c.). The transient thermal impedance curves are also included so that the operating mounting-base temperature can be calculated. Typical SOAR data curves for duty cycles of 0·01, 0·1, 0·2, and 0·5 are illustrated in Figs. 17 to 20. These curves will be used in the examples that follow.

In the few applications (about 10%) which are not covered by the published SOAR curves, the user can derive M_{SB} curves from the single-shot and d.c. SOAR information, and construct the boundaries using the method previously described with reference to Fig. 16.

All Mullard data, including pulsed power ratings, assume the use of square waves and resistive loads. Therefore, the system for using the SOAR and transient thermal impedance curves to be described deals with this type of waveform first, and then methods for other practical cases will be considered. It is assumed that the electrical and time conditions are the fixed parameters of an application at the design stage, and that the thermal conditions can be most easily adjusted. The maximum power must be calculated at the worst-case condition; when the worst-case condition is not obvious, all discrete sets of conditions need to be assessed.

Construction of SOAR using published data

The procedure for constructing a SOAR for one specific set of conditions is described with reference to the curves shown in Figs. 19 and 20, and to the transient thermal impedance curves in Fig. 21.

1) Note the pulse duration t_p (for example, 1·7ms).
2) Note the time between pulses ($T - t_p$) (for example, 2·9ms).
3) Calculate the duty cycle d from the equation $d = t_p/T$ (in this example 0·37)
4) Note the peak collector current I_{CM} (for example 300mA).
5) Note the peak collector emitter voltage V_{CEM} (for example, 35V).
6) Select the SOAR curve with time conditions greater than or equal to the time conditions of the application (in this example, for $d = 0{\cdot}37$ use $d = 0{\cdot}5$ and for $t_p = 1{\cdot}7$ms use $t_p = 2{\cdot}0$ms).
7) Plot the point given by the specific I_{CM} and V_{CEM} values, shown as point Q in Fig. 20.
8) The point Q is acceptable if it is contained within the area of the 2ms/0·5 SOAR as shown in this example.

Thermal calculations

The remaining calculation is one of determining the maximum permissible mounting-base temperature for the application (see Ref. 1). This is achieved as follows.

1) Determine peak power by multiplying I_{CM} by V_{CEM}.
2) Calculate the transient thermal impedance for 1·7ms at 0·37 duty cycle.
   The equation used is:

$$Z_{th(td)} = \{R_{th} - Z_{th(to)}\}d + Z_{th(to)}, \qquad \ldots(5)$$

   where $Z_{th(td)}$ is the thermal impedance for pulse duration t at duty cycle d, and $Z_{th(to)}$ is the thermal impedance for pulse duration t at duty cycle d=0·01 (from Fig. 21).

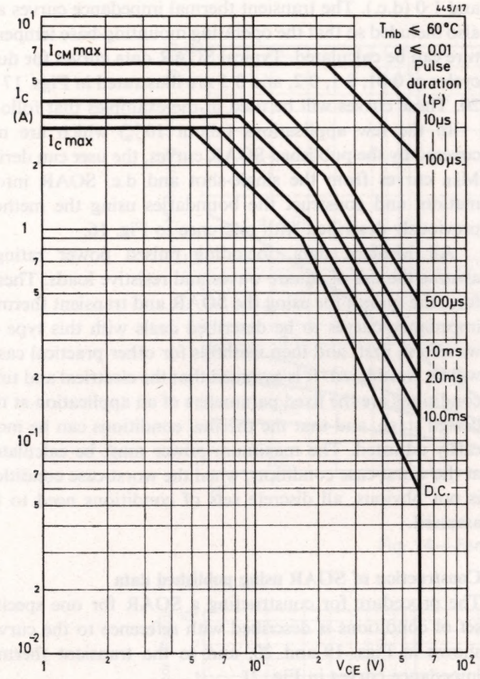

Fig. 17—Typical SOAR family for d ≤ 0·01 (1% duty cycle)

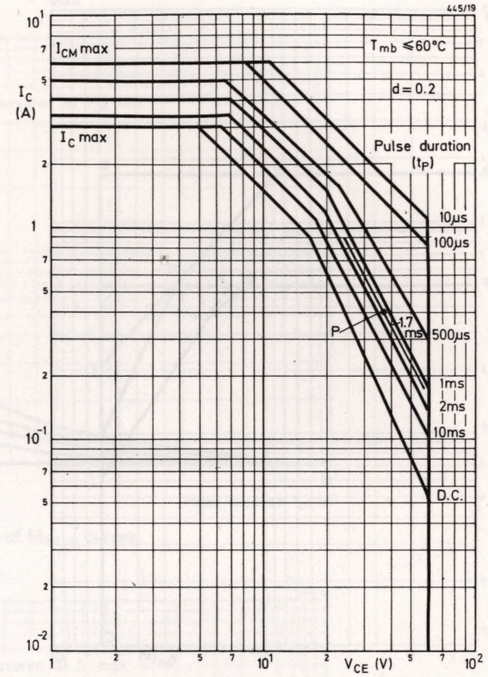

Fig. 19—Typical SOAR family for d = 0·2 (20% duty cycle)

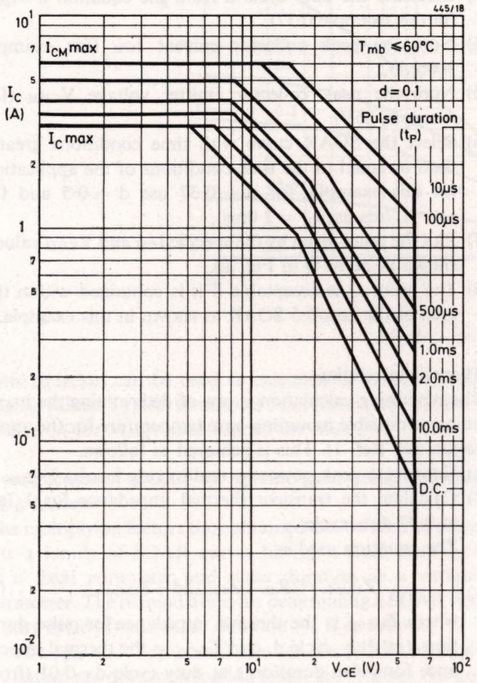

Fig. 18—Typical SOAR family for d = 0·1 (10% duty cycle)

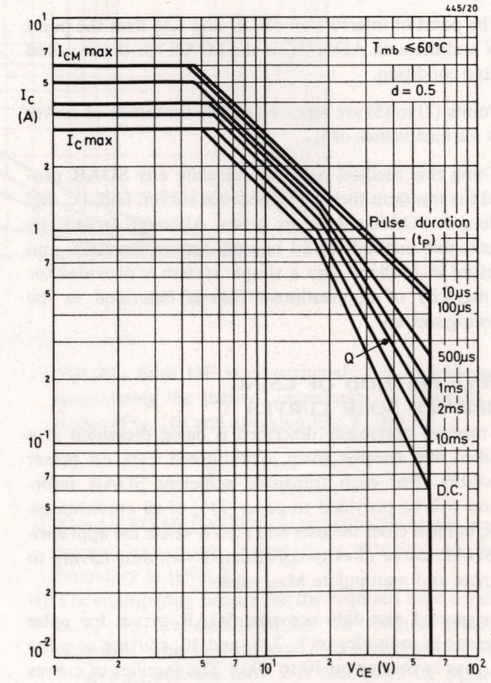

Fig. 20—Typical SOAR family for d = 0·5 (50% duty cycle)

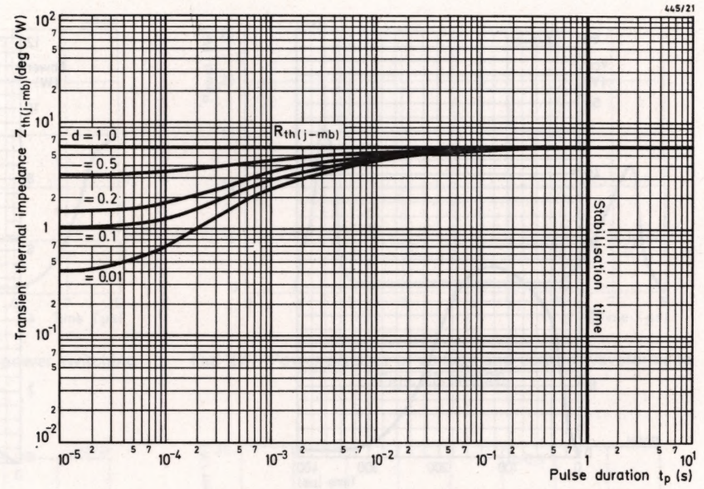

Fig. 21—Family of transient thermal impedance curves for duty cycles from d = 0·01 to 1

3) Calculate the difference between the junction and mounting-base temperature from:

$$(T_j - T_{mb}) = Z_{th(td)} \times I_{CM} \times V_{CEM}. \quad \ldots(6)$$

4) Calculate the maximum permissible mounting-base temperature T_{mb}max from:

$$T_{mb}\text{max} = T_j\text{max} - (T_j - T_{mb}). \quad \ldots(7)$$

5) A heatsink which limits the mounting-base temperature to this value is required. The thermal capacity of the heatsink will be such that the transient effect of the power will be averaged. Hence the thermal resistance is calculated using average power. Thus:

$$R_{th(h-a)} = \frac{T_{mb}\text{max} - T_{amb}}{I_{CM} \times V_{CEM} \times d} - R_{th(mb-h)} \text{degC/W}, \quad \ldots(8)$$

where $R_{th(h-a)}$ is the thermal resistance of heatsink to ambient and $R_{th(mb-h)}$ is the contact thermal resistance.

6) The physical size of the required heatsink can be determined from heatsink published data or from the nomogram in Appendix 1.

Operating outside selected SOAR

Suppose the application had required an I_{CM} of 400mA instead of 300mA. In this case the point P on Fig. 19 would be given. Point P is outside the 2ms area which indicates that the condition may be unacceptable. Thus a closer approximation to the true conditions is necessary.

1) Using linear interpolation between the 1 and 2ms curves at d=0·5 (Fig. 20) draw the SOAR curve for t_p=1·7ms. If point P is within this area then the conditions are acceptable and the heatsink thermal resistance can be calculated.
2) If point P is outside the 1·7ms area, then determine the 1·7ms area on the family of curves for d=0·2 (Fig. 19). A further linear interpolation between the two 1·7ms areas is then needed to approximate to the 1·7ms SOAR at duty cycle of 0·37.
3) If point P is outside this area, then the condition is unacceptable, and a different transistor should be considered.

The above method is not absolutely accurate, but the approximation errors involved are allowed for in the published data tolerances. More accurate calculations can be made by going back to first principles, and calculating the multiplying factor for the specific condition.

Non-squarewave operation

So far only repetitive squarewave pulses in resistive loads have been considered. However, in certain applications repetitive non-squarewave pulses in either resistive or non-resistive loads are used. Thus, it is essential to be able to manipulate these waveforms so that the published SOAR curves, which refer only to squarewave pulses, become applicable.

The most complex form of repetitive non-squarewave is where the current and voltage components are out of phase as in non-resistive loads. The method for finding the appropriate SOAR for such a waveform is described in the following example. This method can also be used when non-squarewave current and voltage components are in phase as in resistive loads.

Example

The out-of-phase voltage and current waveforms shown in Figs. 22 and 23 are to be applied to a power transistor.

The repetition frequency is 750Hz. To determine whether these conditions are acceptable for the device the V_{CE} and I_C waveforms must first be converted into an equivalent squarewave power pulse, as follows.

1) The graph of power against time in Fig. 24 is plotted by taking the product of V_{CE} and I_C.
2) This irregular waveform is converted to a squarewave with the same peak power value with the same area below the curve, as shown by the dashed line in Fig. 24 (see Ref. 1).

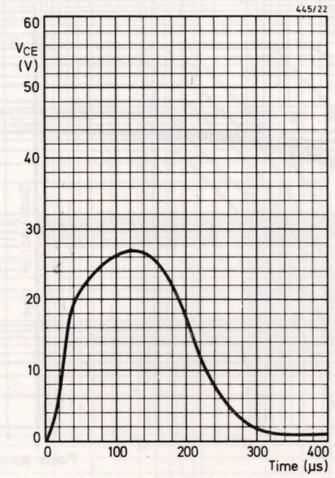

Fig. 22—Non-square out-of-phase voltage waveform V_{CE}

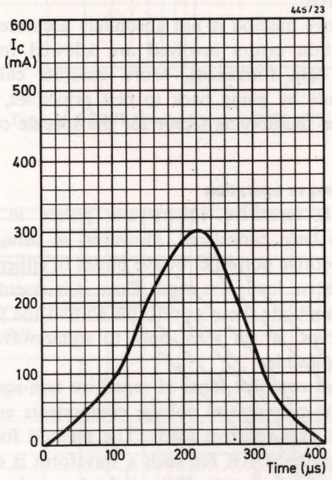

Fig. 23—Non-square out-of-phase current waveform I_C

3) The pulse duration of the equivalent duty cycle is calculated from $d=t_p/T=0{\cdot}081$.
4) The appropriate SOAR curve to suit the time conditions for $d=0{\cdot}081$ and $t_p=108\mu s$ is chosen by the method described for squarewave pulses, where necessary interpolating between families of SOAR curves.
5) On the selected SOAR the locus of the point given by the instantaneous values of I_C and V_{CE} is plotted. If this locus extends beyond any of the four boundaries the SOAR is not acceptable. This locus is plotted because with out-of-phase components of voltage and current it is possible for either I_C or V_{CE} to exceed the maximum peak transistor ratings and yet the power product may remain inside the P_{tot} boundary.

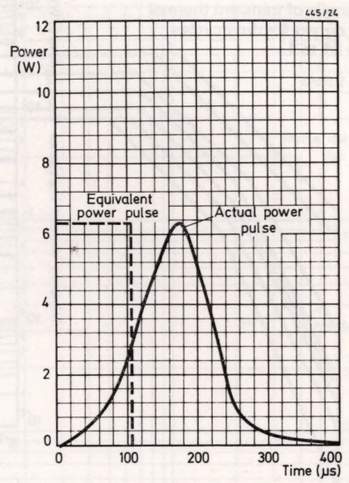

Fig. 24—Power product of V_C and I_C in Figs. 22 and 23: equivalent squarewave with same peak value is shown by dashed line

6) The time and amplitude of the equivalent power pulse are used in the thermal calculations of Eqs. 5, 6, 7, and 8 to determine T_{mb} and hence $R_{th(h-a)}$.

NON-REPETITIVE AND COMPOSITE WAVEFORMS

The application of SOAR curves to repetitive waveforms has been covered in some detail. However, in practice the power transistor is required to handle non-repetitive waveshapes or repetitive power waveforms of a composite nature.

Non-repetitive waveforms

The non-repetitive waveforms occur in applications which have various modes of operation, such as the audio amplifier which may vary from full-load trial with sinewaves down to supplying a low level of background music.

The equivalent squarewaves have to be constructed for each mode of operation. The SOAR and thermal calculations are made and the heatsink is calculated for the condition giving the highest temperature gradient from junction to mounting base.

Composite-power waveforms

Composite-power waveforms exist in power switching applications (for example in an inverter circuit) where switching edges give high peaks of power, and the on and off states give lower levels.

Typical waveforms of current, voltage, and power during inverter switching are shown in Figs. 25 to 27. The duty cycle quoted on these curves (0·5) refers to the complete sequence and not to individual parts of the waveform. The duty cycle system of derating cannot be applied

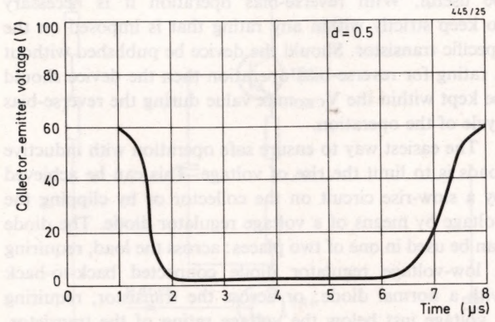

Fig. 25—Collector voltage waveform during power switching

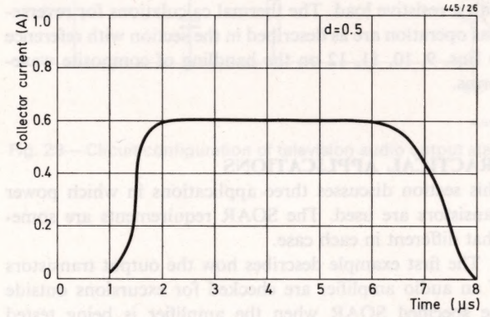

Fig. 26—Collector current during power switching

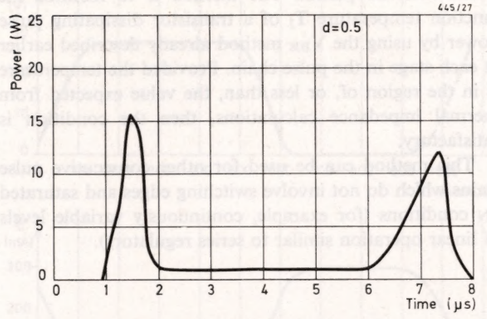

Fig. 27—Power product of voltage and current waveforms in Figs. 25 and 26

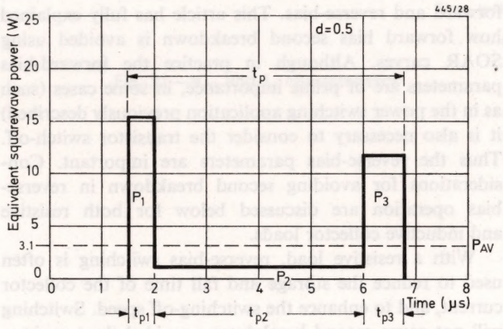

Fig. 28—Equivalent squarewave power with same peak value as in Fig. 27

to composite waveforms, thus a method which uses the graphs at a duty cycle of 0·01 and the average value of power is employed as follows.

The power waveform in Fig. 27 is converted to equivalent-power squarewaves as shown in Fig. 28, and further reduced to an overall average value as also shown in Fig. 28. This gives four levels of power to be manipulated for both heatsink and SOAR calculations.

The heatsink consideration is again one of determining the maximum permissible T_{mb} for the application, and it is found from the following equation:

$$T_{mb}max=T_jmax-(T_j-T_{mb})max, \quad \ldots(9)$$

where:

$$(T_j-T_{mb})max=P_{av}\times R_{th}+\Delta T_j. \quad \ldots(10)$$

ΔT_j in Eq. 10 is the maximum temperature rise of the transistor junction through one complete cycle of pulse power. This temperature rise is calculated as follows:

$$\Delta T_j=(P_1)Z_{th}(t_{p1}+t_{p2}+t_{p3})+(P_2-P_1)Z_{th}(t_{p2}+t_{p3})+$$
$$+(P_3-P_2)Z_{th}(t_{p3}), \quad \ldots(11)$$

or (see Ref. 1) from:

$$\Delta T_j=P_1\times Z_{th}(T_{p1}). \quad \ldots(12)$$

The highest value of ΔT_j from either Eq. 11 or Eq. 12 is used in Eq. 10 to calculate $(T_j-T_{mb})max$ which in turn is substituted in Eq. 9 to find $T_{mb}max$.

The average power line shown in Fig. 28 is found by treating each equivalent squarewave separately. The areas P_1t_{p1}, P_2t_{p2}, and P_3t_{p3} are then added together and multiplied by the factor d/t_p to give the average power; d is the duty cycle of the complete waveform ($d=0{\cdot}5$ for inverters). The $R_{th(h-a)}$ value is calculated but using the average power as shown in Fig. 28 rather than the term ($I_{CM}\times V_{CEM}\times d$).

In power switching applications the second breakdown consideration can often be disregarded. This is because current concentration will not usually occur during short pulses (that is, 10μs or less), or while the transistor is in the saturation mode. However, if the peak powers P_1, P_2, and P_3 approach the SOAR boundaries, second breakdown must be considered since the transistor has a 'thermal memory', and hence the first pulse will affect the second pulse and so on through the power cycle.

The behaviour of consecutive pulses has not been calculated in detail. But if it is assumed that current concentration is dependent on the voltage and current conditions combined with a temperature gradient across the transistor chip, then a method using the additive thermal effects of consecutive pulses can be applied

where facilities permit. The method is to monitor the junction temperature T_j of a transistor dissipating pulse power by using the V_{BE} method already described earlier at each stage in the pulse chain. Provided the temperature is in the region of, or less than, the value expected from thermal impedance calculations, then the condition is satisfactory.

This method can be used for other consecutive pulse trains which do not involve switching edges and saturated ON conditions (for example, continuously variable levels of linear operation similar to series regulators).

REVERSE-BIAS OPERATION

In the introduction, the phenomenon of transistor second breakdown was described in both operational modes; forward and reverse-bias. This article has fully explained how forward bias second breakdown is avoided using SOAR curves. Although in practice the forward-bias parameters are of prime importance, in some cases (such as in the power switching application previously described) it is also necessary to consider the transistor switch-off. Thus the reverse-bias parameters are important. Considerations for avoiding second breakdown in reverse-bias operation are discussed below for both resistive and inductive collector loads.

With a resistive load, reverse-bias switching is often used to reduce the storage and fall time of the collector current, and to enhance the switching-off speed. Switching will not cause second breakdown provided the transistor is operated within the forward-biased SOAR curves during the complete switching cycle.

Reverse-bias second breakdown problems can occur when the V_{CE} is allowed to exceed the V_{CEO} rating. This can happen when switching off transistors with inductive collector loads. The voltage so induced increases the probability of unwanted switch-on in the bulk area of the emitter. The energy dissipated during such a switch-on depends on the current flow prior to the switch-off signal and on the inductance of the load.

The effect of a fixed quantity of energy depends on the reverse-bias conditions which control the emitter area concerned, and the voltage to which the collector is allowed to rise. A secondary factor is the time during which the energy is dissipated.

As a result of these factors, the reverse-bias ratings of a transistor include various selections or combinations of the following parameters in published data:

1) reverse-bias conditions at the base;
2) V_{CE}max during reverse-bias conditions;
3) $I_C$max during reverse-bias conditions, both peak and average;
4) energy level during reverse-bias operation;
5) duration of reverse-bias energy pulse;
6) size of inductive load.

Published data will include reverse-bias parameters which generally cover the intended applications of each device. The following hints on how to avoid reverse second breakdown when using inductive loads should be useful. With reverse-bias operation it is necessary to keep strictly within any rating that is imposed on the specific transistor. Should the device be published without a rating for reverse-bias operation then the device should be kept within the V_{CEO}max value during the reverse-bias cycle of the operation.

The easiest way to ensure safe operation with inductive loads is to limit the rise of voltage. This can be achieved by a slow-rise circuit on the collector or by clipping the voltage by means of a voltage regulator diode. The diode can be used in one of two places: across the load, requiring a low-voltage regulator diode connected back-to-back with a normal diode; or across the transistor, requiring a voltage just below the voltage rating of the transistor.

The energy stored in the inductive load is then dissipated in the regulator diode and not in the transistor. This leaves the transistor to withstand the almost negligible energy comparable with that when switching off with a resistive load. The thermal calculations for reverse-bias operation are as described in the section with reference to Eqs. 9, 10, 11, 12 on the handling of composite waveforms.

PRACTICAL APPLICATIONS

This section discusses three applications in which power transistors are used. The SOAR requirements are somewhat different in each case.

The first example describes how the output transistors of an audio amplifier are checked for excursions outside the specified SOAR when the amplifier is being tested under a sinewave overdrive condition. The second example discusses the special switching requirements of a power transistor used in a converter application, and the third example checks the suitability of an r.f. power transistor used in an s.s.b. driver stage.

Audio application

This example describes how the SOAR curves are used to check the suitability of the BD131 power transistors in a television audio amplifier application. The amplifier is a class A design capable of delivering an output of 2W. The circuit configuration is shown in Fig. 29.

The amplifier provides the required output power but the second breakdown acceptability has to be checked, and the thermal requirements of the heatsinks are to be calculated.

In this example the SOAR acceptability is considered in the event of the transistors being overdriven by a sine-wave signal of period 960μs. A test resistor of 0.1Ω is inserted in the emitter circuit of the lower transistor TR_1. A simultaneous display of the V_{CE} and I_C waveforms is then obtained by connecting the probes of a dual-trace oscilloscope in the manner shown in Fig. 30. The traces of V_{CE} and I_C taken from the oscilloscope are shown in Fig. 31 and the measurements from the waveforms are recorded in Table 1. These readings were recorded every 20μs through the complete cycle of 960μs. In the final column of Table 1, values of instantaneous power are

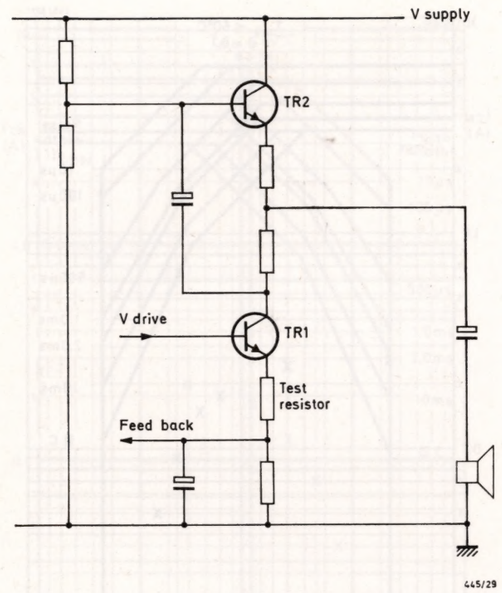

Fig. 29—Circuit configuration of television audio output stage

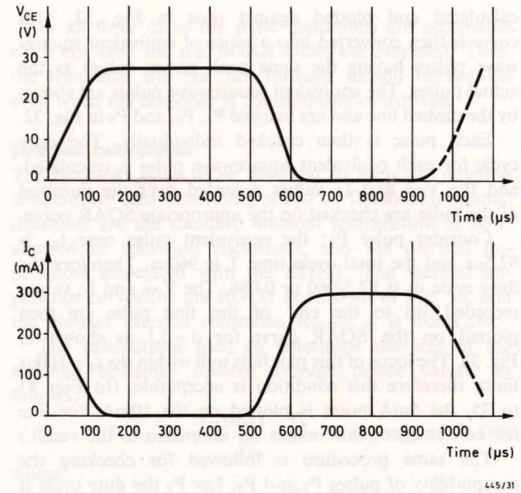

Fig. 31—V_{CE} and I_C characteristics

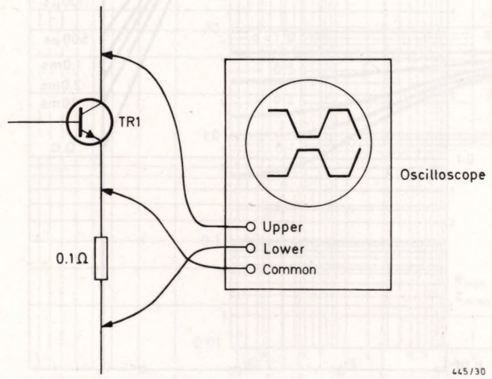

Fig. 30—Method of connecting dual-trace oscilloscope to obtain simultaneous display of I_C and V_{CE}

TABLE 1

Measured values of I_C and V_{CE} and derived $P_{(tot)}$ obtained from oscilloscope display

Time (μs)	I_C (mA)	V_{CE} (V)	$P_{(tot)}$ (W)
0	260	2	0·52
20	220	6	1·32
40	180	12	2·16
60	140	16	2·24
80	90	20	1·80
100	50	25	1·25
120	5	29	0·15
then no important changes until			
500	5	25	0·14
520	40	25	1·00
540	80	20	1·60
560	130	15	1·95
580	180	10	1·80
600	220	5	1·10
620	260	1	0·26
until			
940	280	1	0·28
960	260	2	0·52

calculated and plotted against time in Fig. 32. This curve is then converted into a series of equivalent square-wave pulses having the same peak power values as the actual pulses. The equivalent squarewave pulses are shown by the dashed line and are marked P_1, P_2, and P_3 in Fig. 32.

Each pulse is then checked individually. The duty cycle for each equivalent squarewave pulse is calculated, and the V_{CE} and I_C values recorded over the duration of the pulse are checked on the appropriate SOAR curve.

Consider pulse P_1: the equivalent pulse time t_{p1} is 82.5μs and the total cycle time T is 960μs. Therefore the duty cycle d_1 is 82.5/960 or 0.086. The V_{CE} and I_C values recorded up to the end of the first pulse are then plotted on the SOAR curve for d=0.1 as shown in Fig. 33. The locus of this plot falls well within the t_p=100μs limit, therefore this condition is acceptable. (In Figs 33 to 35, the 5mA point is plotted on the 10mA line line for convenience; this makes no difference to the result.)

The same procedure is followed for checking the acceptability of pulses P_2 and P_3. For P_2 the duty cycle is 420/960 or 0.44; thus the V_{CE} and I_C measurements recorded for pulse P_2 are plotted on the SOAR curve for d=0.5 as shown in Fig. 34. For P_3 the duty cycle is 70/960 or 0.073, so the V_{CE} and I_C measurements recorded for pulse P_3 are again plotted on the SOAR curve for d=0.1 as in Fig. 35.

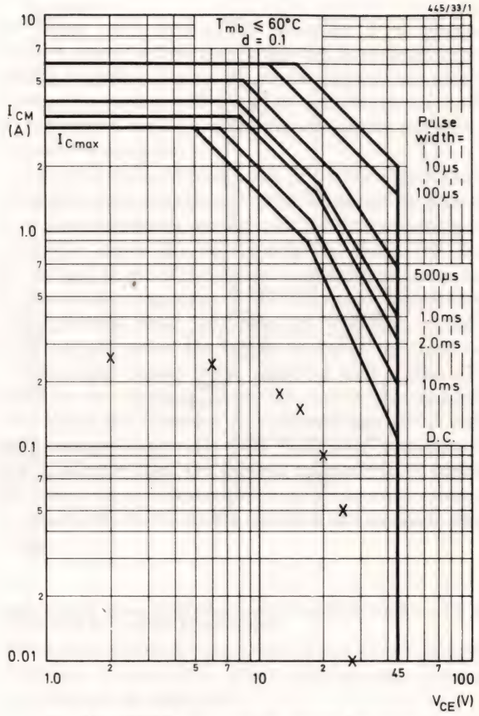

Fig. 33—SOAR acceptability check for pulse P_1

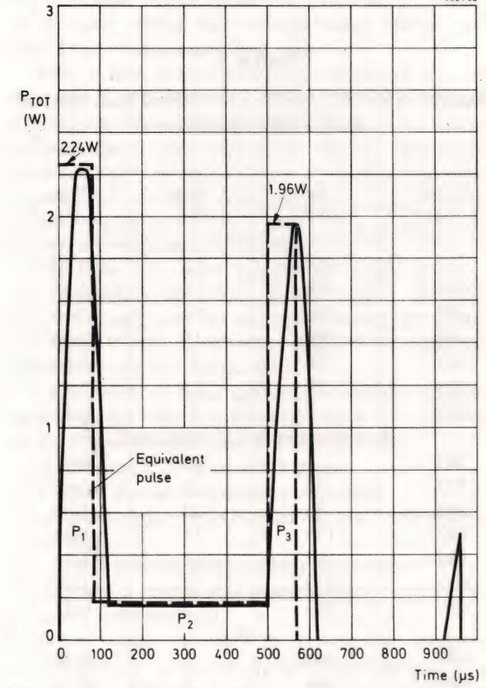

Fig. 32—P_{tot} against time characteristic showing equivalent squarewave pulses

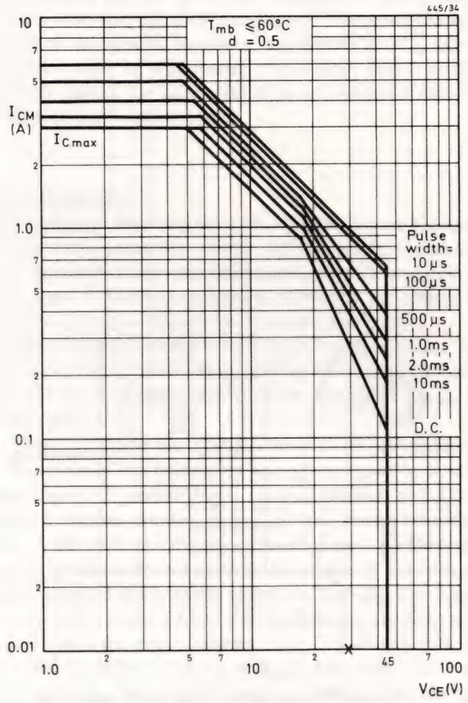

Fig. 34—SOAR acceptability check for pulse P_2

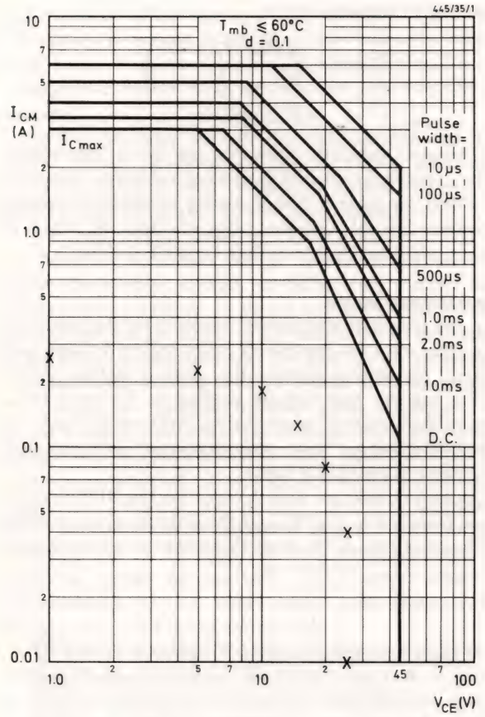

Fig. 35—SOAR acceptability check for pulse P_3

In all three cases the pulse conditions are acceptable since not even the d.c. SOAR limits are exceeded. Thus, the transistor will not fail through second breakdown even when the amplifier is continuously overdriven.

Heatsink calculations

The heatsinks have to be designed to keep the junction temperature below the rating of 150°C. The known thermal restraints are the standard ambient temperature of 60°C allowed in television enclosures, and the thermal impedances associated with the BD131. The thermal impedance curves for the BD131 are shown in Fig. 36, and the contact thermal resistance $R_{th(mb-h)}$ is 1degC/W.

The calculations used to determine the size of the required heatsinks involve average power values, as follows:

$$R_{th(h-a)} = \frac{T_{mb}max - T_a}{P_{av}} - R_{th(mb-h)}, \quad \ldots(13)$$

where:

$$T_{mb}max = T_j max - (T_j - T_{mb})max. \quad \ldots(14)$$

Therefore:

$$R_{th(h-a)} = \left(\frac{T_j max - (T_j - T_{mb})max - T_a}{P_{av}}\right) - R_{th(mb-h)} \quad \ldots(15)$$

Two average powers have to be considered; that during the overload condition and that during the quiescent state. Since this is a class A amplifier, 2W will be dissipated in each of the output transistors during the quiescent condition, and this will be the d.c. bias condition. Under

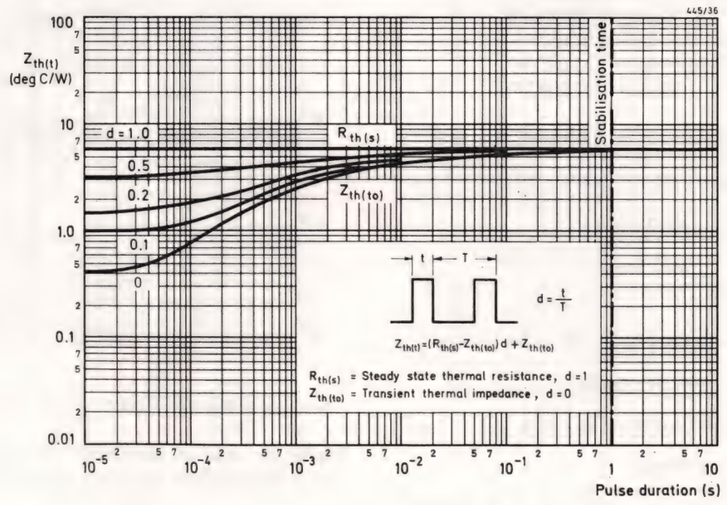

Fig. 36—Thermal impedance curves for BD131

the overload condition the average power value is calculated as follows:
average heat input per cycle

$$=[(t_{p1}\times P_1)+(t_{p2}\times P_2)+(t_{p3}\times P_3)]/T,$$

$$=[(82.5\times 2.24)+(420\times 0.15)+(70\times 1.96)]/960,$$

$$=\frac{385\mu sW}{960\mu s},$$

$$=0.4W.$$

The calculation of heatsink sizes should be determined under worst-case conditions. Generally this occurs when the quiescent state is followed by the overload conditions. Since the average overload power is less than the quiescent power the first cycle of overload will define the $(T_j-T_{mb})max$.

As already described on page 55 the maximum value of $(T_j-T_{mb})max$ is found by substituting, in turn, Eqs. 11 and 12 in Eq. 10 and using the higher value for substitution in Eq. 9. In a similar manner, in this example the two equations corresponding to Eq. 10 are as follows:

$$(T_j-T_{mb})max=P_Q\times R_{th}+(P_1-P_Q)Z_{th}t_{p1}, \quad \ldots(16)$$

and

$$(T_j-T_{mb})max=P_Q\times R_{th}+(P_1-P_Q)Z_{th}(t_{p1}+t_{p2}+t_{p3})$$
$$-(P_1-P_2)Z_{th}(t_{p2}+t_{p3})+(P_3-P_2)Z_{th}t_{p3}, \quad \ldots(17)$$

where:

quiescent power $P_Q=2W$
$P_1=2.24W$
$P_2=0.15W$
$P_3=1.96W$
$t_{p1}=82.5\mu s$
$t_{p1}+t_{p2}+t_{p3}=572.5\mu s$
$t_{p2}+t_{p3}=490.0\mu s$
$t_{p3}=70\mu s$
$R_{th}=6degC/W$
$Z_{th}t_{p1}=0.72degC/W$
$Z_{th}(t_{p1}+t_{p2}+t_{p3})=2.0degC/W$
$Z_{th}(t_{p2}+t_{p3})=1.8degC/W$
$Z_{th}t_{p3}=0.63degC/W.$

Thus, Eq. 16 becomes:

$$(T_j-T_{mb})max=(2\times 6)+(0.24\times 0.72),$$

$$=(12+0.2),$$

$$=12.2degC.$$

Eq. 17 becomes:

$$(T_j-T_{mb})max=(2\times 6)+(0.24\times 2)-(2.09\times 1.8)+$$
$$+(1.81\times 0.63),$$
$$=12+0.48-3.76+1.14,$$
$$=9.9degC.$$

Therefore the maximum value of (T_j-T_{mb}) is 12.2degC from Eq. 16.

Thus Eq. 15 becomes:

$$R_{th(h-a)}=\left(\frac{150-12.2-60}{2}\right)-1,$$
$$=37.9degC/W.$$

Therefore heatsinks used for the BD131 transistors in this application should each have a thermal resistance of 37degC/W or less. The foregoing calculations assume a contact thermal resistance value of 1degC/W, which is true only if a heatsink mounting compound is used.

Converter application

In many converter and inverter applications the switching transistor must be capable of withstanding voltage and current excursions outside the normal SOAR limits during turn-on and turn-off operations. To meet these requirements special inverter-grade transistors, such as the BDY90 series, have been developed with specified extensions to the SOAR limits.

As an example, an SOAR curve for the BDY93 transistor is shown in Fig. 37 and the extensions are marked by the areas III and IV. Area IV allows the voltage across

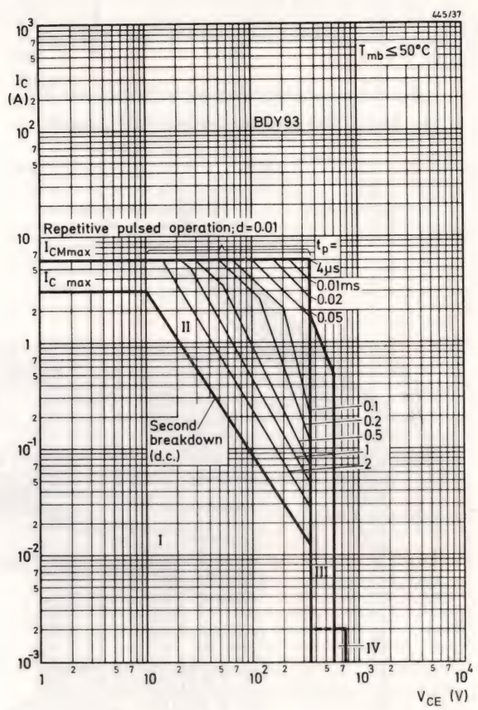

Fig. 37—SOAR curve for BDY93

Region III: area of permissible operation during turn-on in single-transistor converters, provided $t_p \leq 0{\cdot}6\mu s$ and $R_{BE}\leq 100\Omega$
Region IV: repetitive pulse operation in this region is allowable provided $V_{BE}\leq 0$ and $t_p \leq 2ms$

the transistor to increase up to 750V at turn-off provided the current is reduced to less than 2mA before the voltage rises above $V_{CEO}max$. Area III permits turn-on from a voltage in excess of V_{CEO} provided the time condition is observed.

In the following example a basic flyback converter circuit already described in Ref. 2 is further considered from the point of view of its modification to meet the SOAR requirements of the switching transistor.

The basic flyback converter circuit is shown in Fig. 38. To limit the maximum voltage across the transistor to twice the supply voltage, an additional winding and diode can be employed, as shown in Fig. 39. This winding returns the energy stored in the inductance to the supply if the circuit is operated with no load on the secondary. The additional winding is bifilar wound with the primary to ensure low leakage between these windings. The extra winding also limits the amplitude of the voltage spike at the transistor collector which can occur when the transistor is switched off and there is appreciable leakage inductance between the primary and the secondary. Note that the diode is connected in series with the high potential end of the bifilar winding so as to avoid the collector current turn-on spike which would otherwise be produced by the interwinding capacitance if the diode were placed in the earthed end.

To keep the transistor within its safe operating area, it is normally necessary to ensure that the collector current is reduced to zero before the collector voltage is allowed to rise above the V_{CEO} rating of the transistor.

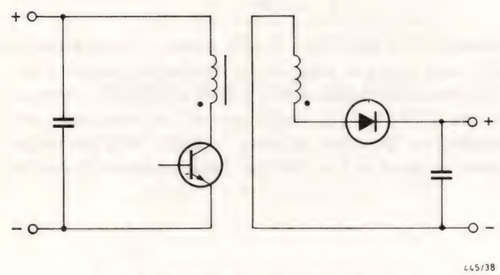

Fig. 38—Basic flyback converter circuit

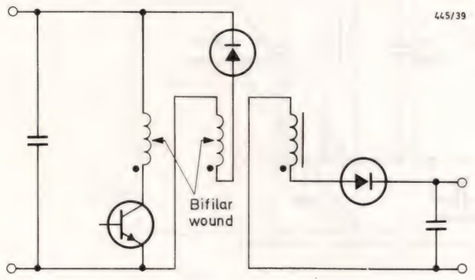

Fig. 39—Flyback converter with voltage limiting circuit

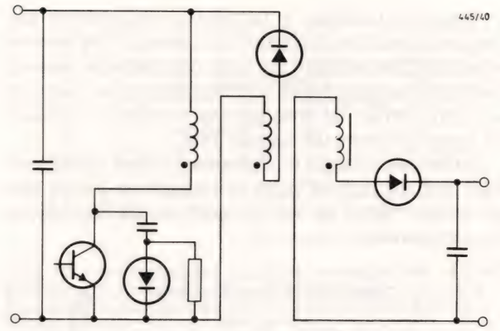

Fig. 40—Flyback converter with added 'slow-rise' circuit

Therefore if the V_{CEO} rating is not greater than twice the maximum supply voltage, additional circuitry must be inserted to slow down the rise of collector voltage. This additional 'slow-rise' circuitry is included in Fig. 40. When the transistor is switched off, the transformer current is diverted into the capacitor which charges through the diode. The capacitance value is chosen such that the rise of the collector voltage is slowed down as required.

The I_C versus V_{CE} locus for the BDY93 transistor during turn-off, with and without the 'slow-rise' circuitry, is shown in Fig. 41. With the inclusion of the slow-rise circuit operation is kept within the SOAR limits.

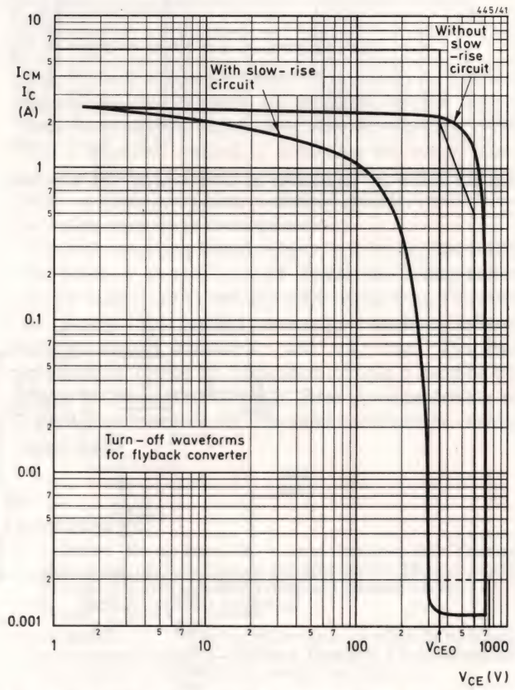

Fig. 41—Turn-off waveforms for BDY93 with and without slow-rise circuitry

When the transistor is turned on, the capacitor discharges through the transistor and resistor. The resistor value must be sufficient to limit the discharge current, thus avoiding an excessive current spike in the transistor as shown in Fig. 42. With too low a value of resistance the current is above the I_{CM}max limit.

In this type of circuit it is advisable to check the turn-on pulse and the turn-off pulse individually to ensure that the relevant limits are not exceeded for the appropriate pulse-duration and duty cycle.

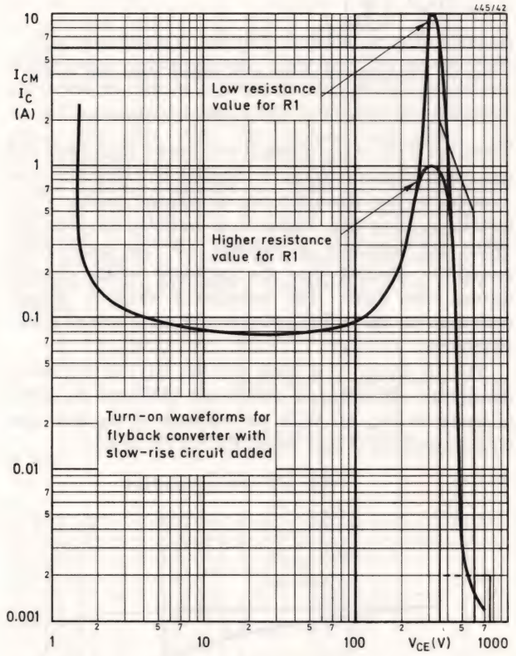

Fig. 42—Turn-on waveforms for BDY93 with high and low values for resistor in slow-rise circuit

R.F. power application

In r.f. power applications the problem of second breakdown is of importance; however, greater importance must be attached to the need to control the heatsink temperature T_h with power dissipation. In the published data on v.h.f. and u.h.f. power transistors, d.c. SOAR curves are given with the P_{tot} boundary specified at a certain T_h value. Other curves for r.f. power transistors include P_{tot} against T_h, and load power P_L against v.s.w.r.

In this example a BLX13 v.h.f. transistor is used in an 8W broadband s.s.b. driver amplifier operating in class A. The bandwidth of the amplifier is 1.6 to 30MHz and the intermodulation product at 8W is better than 40dB. Full circuit details and performance figures have been published in Ref. 3. The object of this example is merely to show that the BLX13 transistor is being operated within its SOAR limits.

The circuit diagram of the amplifier is shown in Fig. 43 and the circuit layout in Fig. 44. The supply voltage is 28V and the maximum allowable heatsink temperature is taken to be 70°C maximum. A voltage drop of 2V across the emitter resistor R_5 results in a voltage V_{CE} across the transistor of (28−2)V or 26V.

From the d.c. SOAR curve in Fig. 45b, at a maximum heatsink temperature of 70°C and with 26V across the transistor, the maximum permissible current is 1.075A. In class A operation the maximum output power P_o is equal to one half of the d.c. input power. Therefore:

$$P_o=(I_C\times V_{CE})/2,$$
$$=(1.075\times 26)/2,$$
$$=14\text{W}.$$

However, the maximum output power is approximately 20% less, owing to losses in the feedback network L_1R_1. Thus the actual output power is further reduced to between 11 and 12W. At this output power the measured intermodulation distortion is below −30dB. With the output power reduced to 8 or 9W the intermodulation distortion

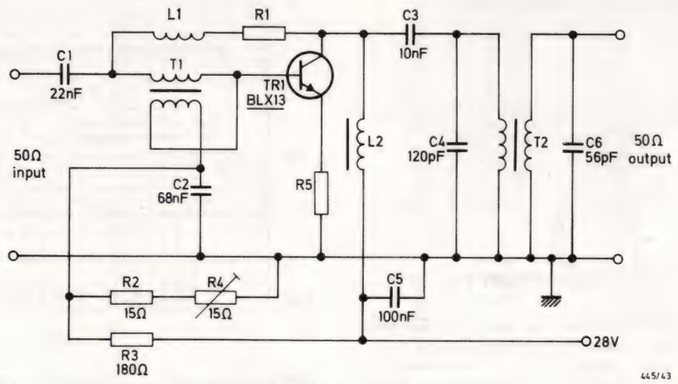

Fig. 43—8W p.e.p. class A driver

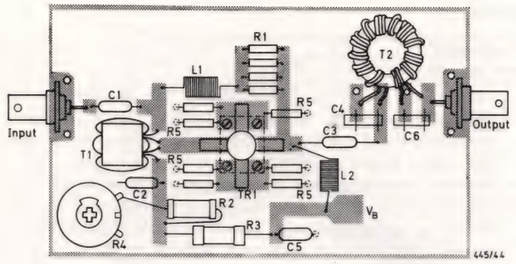

Fig. 44—Circuit layout of 8W p.e.p. class A driver

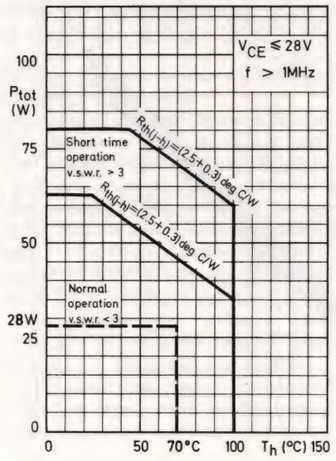

Fig. 45a—P_{tot} against T_h for BLX13

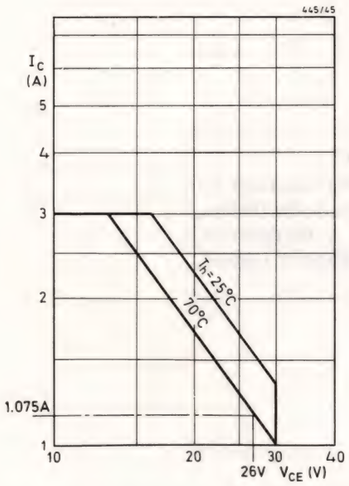

Fig. 45b—D.C. SOAR curves for BLX13

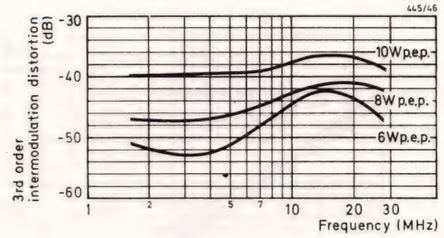

Fig. 46—Intermodulation distortion plotted against frequency for three output power levels

improves to better than −40dB, as shown in Fig. 46.

The curve shown in Fig. 45a gives P_{tot} against T_h. From this curve it can be seen that for maximum output of between 11 and 12W the transistor dissipation of 28W with a heatsink temperature of 70°C is perfectly acceptable. The operating point falls well within the ratings for normal operation of the transistor. Therefore, the transistor is acceptable for this application.

CONCLUSIONS

Three questions are sometimes asked about SOAR:

1) How can one determine what thermal impedance to use on or near the second breakdown limited area?

2) How does one convert the single family of SOAR curves at 10% or 1% duty cycle to an application at 37% duty cycle?

3) Is there an easier way of using SOAR?

The Mullard system is based on a family of thermal impedance curves, which are protected by the second breakdown ratings. The data includes various duty cycles with a simplified method of expanding the range. Alternatively the SOAR can be constructed from first principles. Both methods have been described in this article, thus providing answers to these questions.

SOAR is a complicated subject, but by understanding the Mullard system, second breakdown acceptability can be determined in the shortest possible time. Provided the ratings are applied correctly, transistor failures through second breakdown will not occur. The best argument in favour of this system is that it enables the ratings to be applied correctly. Also the acceptability of a particular transistor for the application can be rapidly determined.

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2. Jansson, L. E., 'A Survey of converter circuits for switched-mode power supplies'. **Mullard Technical Communications,** Vol. 12, No. 119, July 1973, pp 271 to 278.

3. 'Transistors for single-sideband linear amplifiers', TP1337, Mullard Ltd., 1972.

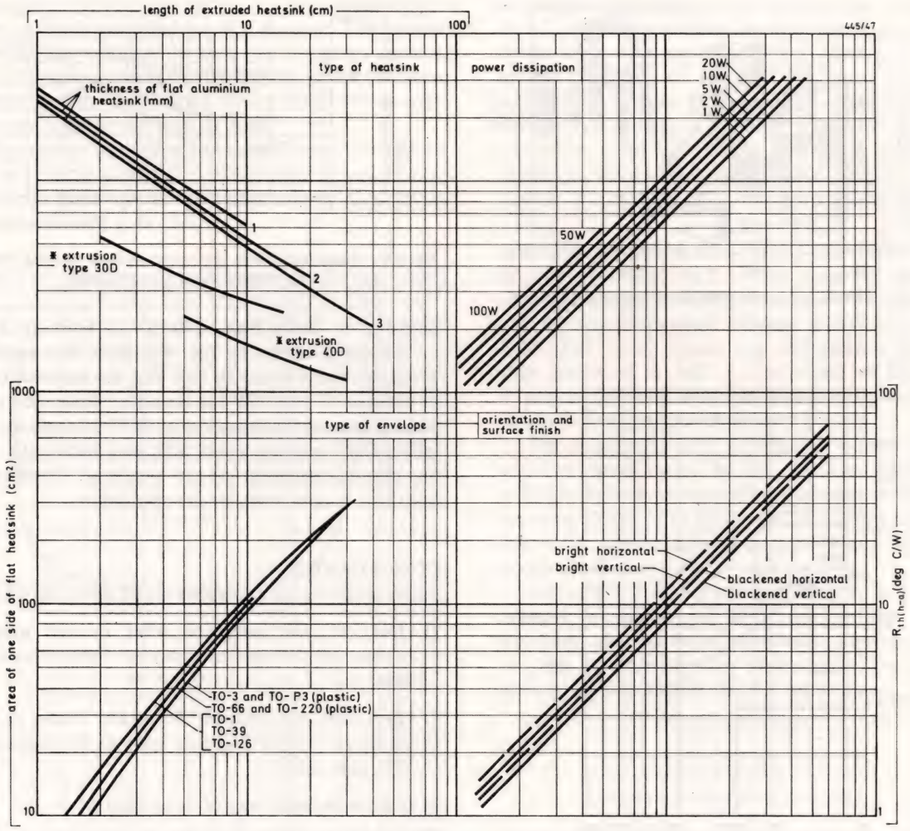

Fig. 47—Heatsink nomogram. *(For outlines of extrusions see Fig. 49)

ACKNOWLEDGEMENTS

The authors wish to thank the following colleagues for help in the creation of this article: W. van de Pol (Philips, Nigmegen), R. S. Babbs, M. D. Brett, J. A. Houldsworth, L. E. Jansson, N. van Vliet (all of Mullard Limited, Mitcham).

APPENDIX 1

Transistor heatsink sizes

The heatsink size for any transistor can be found from the nomogram shown in Fig. 47 provided that the power dissipation is no greater than 100W, and that the heat is dissipated by free convection. This nomogram should not be used where forced air cooling is employed, or where heatsink material other than aluminium is desired. The nomogram is operated as follows, with reference to the simplified curves in Fig. 48.

1) Calculate the worst-case dissipation P_{tot}max and hence the thermal resistance of heatsink to ambient $R_{th}(h-a)$. Thus:

$$R_{th(h-a)} = \frac{T_{mh}max - T_{amb}}{P_{tot}} - R_{th(mb-h)}$$

2) Enter the nomogram in section I of Fig. 48. Move horizontally to the left until the appropriate orientation (either horizontal or vertical) and the appropriate surface finish is reached.
3) Move vertically upwards to intersect appropriate power dissipation curve (P_{tot}) in section II.
4) Move horizontally to intersect the curve in section III for the desired thickness of sheet aluminium heatsink. If an extrusion is required, move vertically upwards from the point of intersection on the chosen extrusion curve and read off the required length on the top horizontal scale. (The 30D and 40D are shown in outline in Fig. 49. These types belong to the family of extrusions which has been used with Mullard power devices requiring special heatsink considerations, such as thyristor stacks and power rectifiers. Similar curves for alternative extrusions could also be plotted in section III using the heatsink manufacturer's data relating $R_{th(h-a)}$ and power, and length).
5) Move vertically down from point A in section III to intersect with the appropriate curve for the transistor encapsulation style.
6) Move horizontally to the left and read off the required area of one side of flat aluminium heatsink.
7) The heatsink dimensions of height to width should not exceed the ratio 1·25:1.

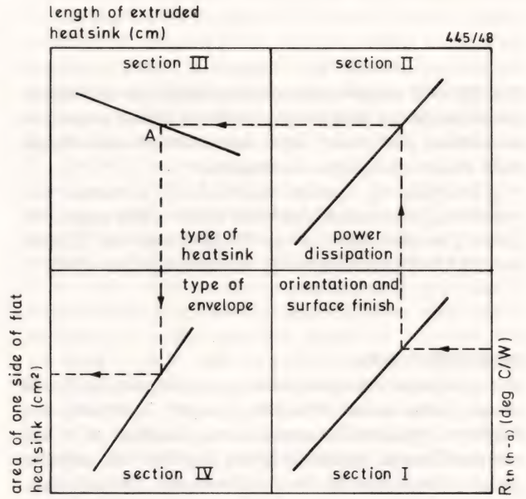

Fig. 48—Simplified nomogram

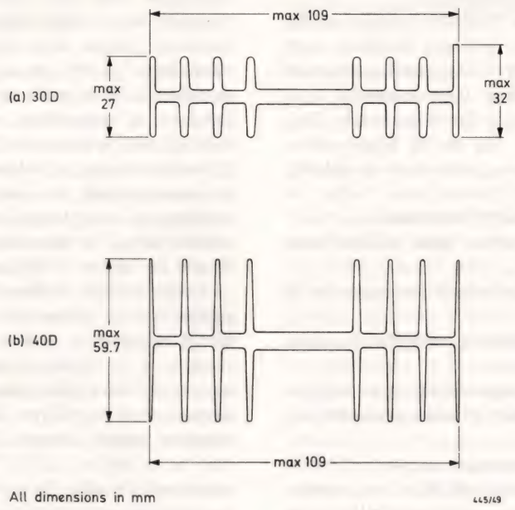

Fig. 49—Outlines of extrusions: (a) 30D, (b) 40D

Economical RGB colour decoder with three ICs

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UDC 621.397.132 [621.382]

The TCA800 colour synchronous demodulator and matrix integrated circuit enables an economical colour decoder to be realised with three 16-pin integrated circuits. Simple RGB video output stages are employed.

The results of detailed study of d.c. tolerances and operational drifts associated with simple video stages are given. The application of the TCA800 with the TBA540 and TBA560C in a complete decoder circuit is described.

INTRODUCTION

The established first-generation colour decoder integrated circuits comprise the TBA530, TBA540, TBA560C, and TBA990. The TBA530 combines the functions of Y and colour-difference signals matrixing together with negative signal feedback over the video output stages. This technique, with each video output transistor contained inside a feedback loop that has a very high basic gain figure, has proved itself to have very good d.c. stability and linearity. In the interests of cost reduction and the general improvement in reliability that can be expected by reducing the component count, a simpler system, not employing feedback over the output stages, has been produced.

A new integrated circuit, the TCA800, contains all the colour demodulation and PAL switching functions, with internal RGB output amplifiers incorporating clamped d.c. feedback, and it provides large-amplitude low-impedance stable drive signals for the video stages. This enables very simple low-gain (20 to 25 times) video output stages to be used having minimum complexity and low inherent d.c. drifts.

The advantages offered by the TCA800 are:

a) The complete decoder comprises three 16-lead integrated circuits.
b) A substantial saving in peripheral components is afforded.
c) The option is given of dispensing with the d.c. level adjustments of the drive signals.
d) A choice of video stage design according to requirements of d.c. stability, method of white point setting, etc., is permitted.
e) The decoder current consumption is reduced.

This article describes a complete RGB colour decoder using established PAL techniques and employing three integrated circuits: the TBA540, TBA560C, and TCA800. It is designed to process a composite video signal of 3V peak amplitude supplied by the TCA270 synchronous video demodulator integrated circuit, and provides RGB drive signals to the picture tube. The general requirements for the integrated circuit decoder are first discussed.

ENVIRONMENTAL CONDITIONS FOR INTEGRATED CIRCUITS

Integrated circuits are similar to discrete semiconductor devices in their requirements for particular environmental conditions to ensure safe and reliable operation in television receivers. In both cases, ambient temperature variations, supply voltage variations, and protection against voltage surges and picture tube flashover energy, require similar consideration. However, there are certain special requirements for integrated circuits, particularly where several devices may be used together in a receiver.

Power supplies

The design of each of the integrated circuits allows at least $\pm 10\%$ voltage range over which correct operation is maintained. As a general design approach most of the signal amplitudes, d.c. levels, and control functions associated with each integrated circuit track proportionately with voltage. However, in a receiver with well-stabilised picture tube supply potentials, an operational variation of $\pm 10\%$ in supply voltage to the integrated circuits is likely to result in unacceptable picture variations. Because of operational variations of mains voltage, ambient temperature, and picture tube beam current, an l.t. supply having a voltage stability tolerance of $\pm 3\%$ is recommended to ensure a high degree of picture stability. In any design, however, the operational variations, added to the set-to-set spread in supply voltage, should lie within $\pm 10\%$ of the nominal supply voltage.

Unlike groups of discrete components, where the total supply current consumption is the result of an average of the effects of a number of components, all the components of the same kind in an integrated circuit can vary above or below the nominal case together. Integrated circuits of a given type therefore exhibit a tolerance in required supply current (at a constant voltage) which may be as high as $\pm 25\%$. In a system comprising several integrated circuits there is therefore the possibility of considerable variation in total current demand from one assembly to another. This must be allowed for in the design of the power supply circuit.

An 18 to 24V l.t. supply is usually available in an all-transistor receiver, and it is convenient to provide the power for the integrated circuits from this. Total current for the decoder is typically 160mA $\pm 20\%$. The requirement for good tracking of the supply potentials to each integrated circuit, together with the tolerances in current demand for each one, generally precludes the operation of the integrated circuits from the l.t. rail via individual voltage-dropping resistors. Furthermore, similar operation but with a common voltage-dropping resistor would also be unacceptable because of the possibility of a combination of one high-current integrated circuit with a number of low-current ones. The result could be that the voltage across all the circuits would be considerably higher than nominal, and excessive power dissipation could occur in the high-current circuit.

These conditions lead to the requirement for:

1) a simple supply source having adequate voltage stability and low impedance, or
2) a resistor feed with a single parallel voltage reference diode connected across the integrated circuits, or
3) a series stabiliser employing a transistor with a voltage reference diode.

For (1), a direct scan-rectified 12V supply could be obtained from the line output transformer in an all-transistor receiver. Such a supply would have voltage variations due to beam current of typically 0·6V for 90° deflection circuits and 0·3V for 110°. However, a diode, an electrolytic capacitor, and an extra transformer tap would be required as well as flashover protection components, and so this is not necessarily the most attractive solution.

For (2), a single voltage reference diode of about 1W dissipation would be required with a $\pm 5\%$ voltage tolerance, and for (3) a series transistor (BD131) regulated by a small voltage reference diode and possibly a preset potentiometer. Solution (2) has been used in the decoder circuit described here.

Power supply surges and protection from picture tube flashover energy

Although it is unlikely that surges of any significance will occur during normal operation with a stabilised supply voltage, consideration must be given to the safety of the integrated circuits in the event of a possible fault condition. The most hazardous occurrence is failure of the stabilising device. In the case of a parallel-connected voltage reference diode it is unlikely that an open-circuit will be caused by damage; a short-circuit is more likely. Where a series stabiliser transistor is employed, which could, for example, be overloaded by a short-circuit on the 12V line, a combination of a series current-limiting resistor and a transistor that will not be damaged by the surge current gives adequate protection.

Generally, the integrated circuits will not be affected by surges in supply voltage up to 50% higher than the nominal, provided that each surge is limited to about 20s duration.

Integrated circuits require the same attention to design and layout as discrete transistors to ensure adequate protection against circulating currents caused by picture tube flashover discharges. Where pulses from the line and field timebases are employed for the various gating functions, the layout of the associated networks and the types of components used must not permit the transfer of sharp voltage spikes. Similar attention must be given to the power supply network, particularly if this is derived from the line output transformer.

As with any semiconductor circuitry, it is of prime importance to ensure that any wires or cableforms which carry control potentials or signals associated with the integrated circuits are kept away from the picture tube. The external Aquadag coating and the rimband of the picture tube can be dangerous sources of flashover energy. A particular situation which must be avoided is where the channel selection mechanism and receiver controls are mounted on a panel closely adjacent to the band. A clearance of at least 30mm between such metalwork and the band is recommended, and the control wiring must be positively located in such a way that it cannot come close to any part of the picture tube. As a further precaution, a series resistor, situated close to the IC, is recommended to be connected to any long lead to ensure complete protection against flashover effects. For normal d.c. control leads a value of 1kΩ is appropriate. However, in the case of long leads carrying pulses or signals, a lower value may be necessary to avoid waveform distortion. Provided that the leads in such cases are not excessively long, a value of 100Ω gives useful protection. Each integrated circuit should have a bypass capacitor (typically 100nF, metallised-film type) connected close to its supply pins to give stability and isolation at high frequency. These capacitors also increase the protection of the integrated circuits against flashover effects.

Heat considerations

When the decoder supply voltage is determined by a $\pm 5\%$ tolerance voltage reference diode, as described here, the integrated circuits are permitted to operate up to a cabinet ambient temperature of 55°C.

Layout requirements

An integrated circuit, owing to the large number of active devices usually contained on the chip, can have a very high power gain between its input and output circuits. In this respect, the layout of the decoder panel is rather more critical than with discrete transistors. Interference between high- and low-level circuits of different channels can occur unless sufficient attention is given to avoiding common paths and coupling loops in the layout. Experience has shown that, with integrated circuits, a layout following a pattern of earth loops or boxes intended to improve isolation between different circuits is unsatisfactory. A branch pattern for the earthing of the various channels is better. This allows the earth paths for the luminance, chrominance, and reference signal channels to converge and meet at the RGB output circuit. Individual bypass capacitors of about 100nF should be connected across the supply terminals of the integrated circuits to provide adequate decoupling.

Radiation of harmonics of the 4·43MHz components in the demodulated colour-difference signals is minimised

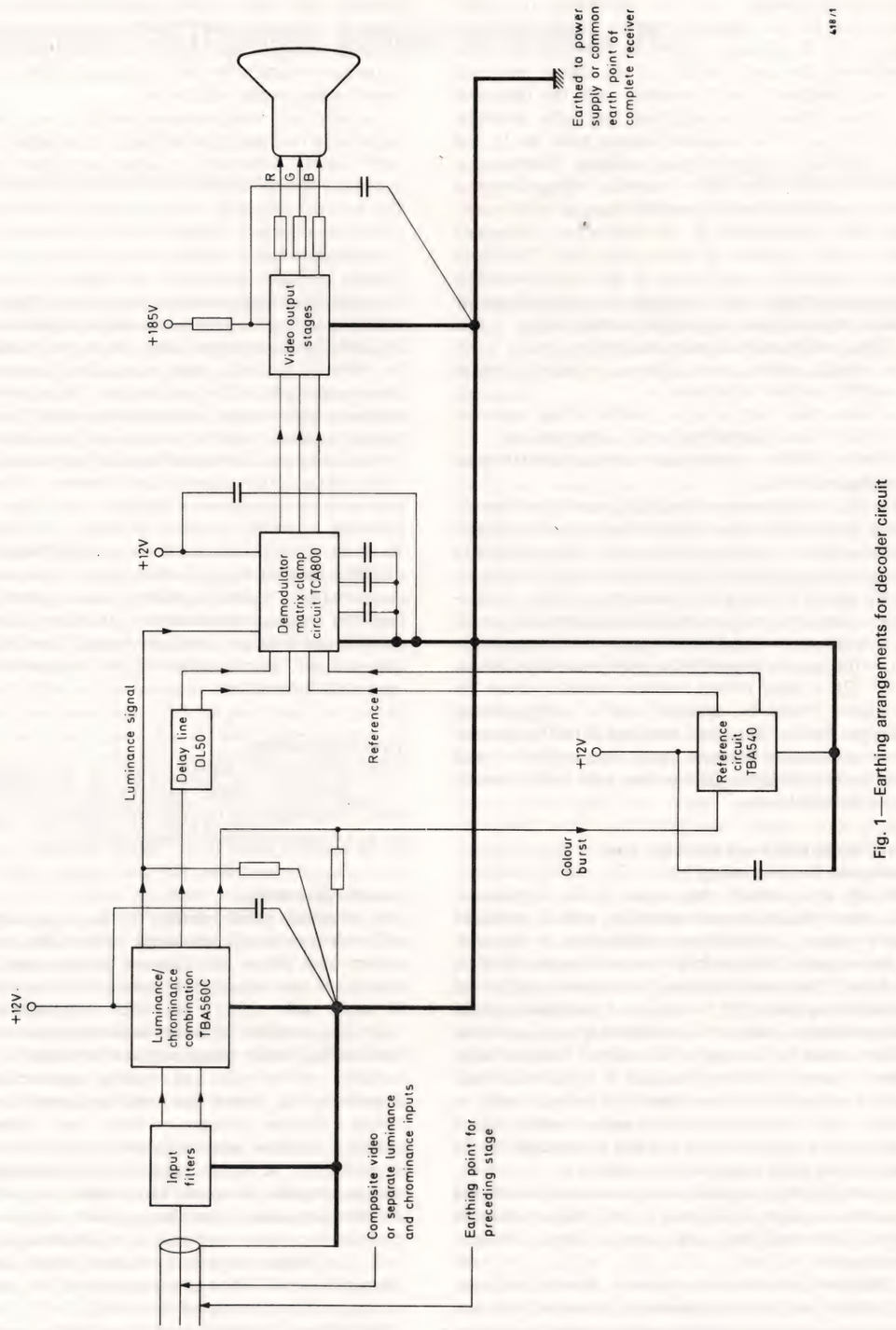

Fig. 1—Earthing arrangements for decoder circuit

by the lowpass filters integrated in the TCA800. Nevertheless, radiation of the products of demodulation from the picture tube drive signal leads can occur, and series resistors connected close to the output transistors are usually found necessary.

A typical recommended layout of the main earth and signal paths is illustrated in schematic form in Fig. 1. Each block includes the appropriate integrated circuit with its peripheral components. The earth point for each block should be as close to the earth pin of the integrated circuit as possible. Note that the chrominance and reference signals do not have common earth paths before detection (by the TCA800), hence crosstalk is minimised. If the necessity for decoupling chokes in the 12V supply circuit is to be avoided, there must similarly be no common paths in the 12V supply lines to the reference and chrominance circuits before the TCA800. Finally the earth track from the TCA800 is taken to the earthing point of the RGB video output stages, and this point is used as the common earth point for the complete decoder circuit.

SYSTEM DESCRIPTION

The colour decoder uses standard PAL processing functions and is shown in the block diagram (Fig. 2). The signal paths, as distinct from control function paths, are shown as bold lines.

In accordance with established practice, an a.c. coupled and d.c. clamped luminance channel is employed. The input to the decoder may be composite video, or separate luminance and chrominance signals (luminance signal amplitude into the TBA560C = 0·4mA black-to-white) and the outputs from the RGB stages are 100V black-to-white amplitude.

The detailed requirements of each integrated circuit in relation to its operation with its peripheral components are described in the published data. The following description deals with the overall operation of the decoder.

DECODER CIRCUIT DESCRIPTION

The complete decoder circuit diagram and all test references are shown in Fig. 3.

The input circuit of the decoder is arranged to accommodate a composite video input from either an i.f. amplifier equipped with a synchronous demodulator or from a video distribution system. Alternatively, separate luminance and chrominance inputs, for example from an i.f. amplifier with separate diode detectors, can be used.

The luminance signal can be supplied, for example, from the TCA270 video synchronous demodulator IC. This has a black-to-white amplitude of 1·7V which is applied, via a 6MHz sound carrier filter and delay line terminating resistors R_7 and R_8, to the luminance delay line (R_o = 1·5kΩ). A luminance delay of about 500ns has been found to be the optimum for the complete decoder described, but the actual value required in a particular circuit will depend on such factors as chroma filter bandwidth and the i.f. amplifier response. The total series resistance network in the luminance signal input circuit provides the required TBA560C input signal current of 0·4mA black-to-white amplitude.

The chroma trap L_1 C_8 C_9 is designed to give a high rejection at 4·4MHz (20dB) consistent with a narrow 3dB bandwidth (±500kHz) and negligible distortion of the 2τ pulse. The luminance signal is a.c. coupled by C_{15} into the TBA560C. A d.c. bias current of 1·0mA is also fed into pin 3, via R_{16}, from the +12V line.

The chroma input to the TBA560C is supplied from the composite video input signal via a chroma filter network.

Pulse shaping circuit

A positive-going pulse is needed on pin 10 of the TBA560C for the colour-burst gating and black-level clamping functions. This is obtained as follows. A winding on the line output transformer supplies a +27V pulse having a mean level of 0V and this is applied to pin 10 via R_{25}, R_{26}, D_2, and C_{17}. During the line scan period the charge potential on C_{18} is about 0V. The arrival of a flyback pulse causes D_2 to cease conduction, and the potential across C_{18} rises exponentially as it charges via R_{28} towards +12V. When the trailing edge of the flyback pulse voltage becomes equal to the voltage to which C_{18} has charged, D_2 again conducts and discharges C_{18}, returning the potential on C_{18} to 0V. The instant of conduction of D_2 is determined by the flyback pulse amplitude and is therefore adjustable by R_{26}*. Thus a positive-going sawtooth waveform of 3·5V peak-to-peak amplitude, whose duration is slightly less than that of the flyback pulse, is developed across C_{18}. This waveform is coupled via C_{17} to pin 10 of the TBA560C. There is a diode characteristic on this pin so that conduction occurs only during the tip of the sawtooth waveform. The input current to pin 10 operates the luminance clamp and burst gate circuits, and so the timing and duration of these functions can be determined by the choice of values for R_{28} C_{18}.

Negative-going pulses for line and field flyback blanking in the luminance channel are required on pin 8. To avoid the need for a second line timebase pulse to the decoder, and also because a positive-going pulse is more readily obtainable from common designs of field timebase, a transistor is employed to develop suitable pulses. Transistor TR_1 is non-conducting during the line scan period and saturated for most of the duration of the line flyback pulse because R_{42} has a relatively low value. The network R_{34} R_{40} is arranged to provide the correct amplitude of blanking pulse, which is then coupled to pin 8. The field blanking pulse of 30V peak-to-peak amplitude is applied, via R_{43} and C_{29}, to TR_1. The value of R_{42} is chosen to give a sufficiently long duration of field blanking pulse. In a case where a negative-going field flyback pulse is available, it could, of course, be a.c. coupled directly to pin 8 of the TBA560C but its amplitude must not be greater than

*The phase performance of the receiver's line flywheel system must be taken into account in determining the nominal phase position of the gating pulse. In a complete receiver having not more than ±0·5μs phase deviation over the working range of the line flywheel system, it should be possible to replace R_{26} with a fixed resistor.

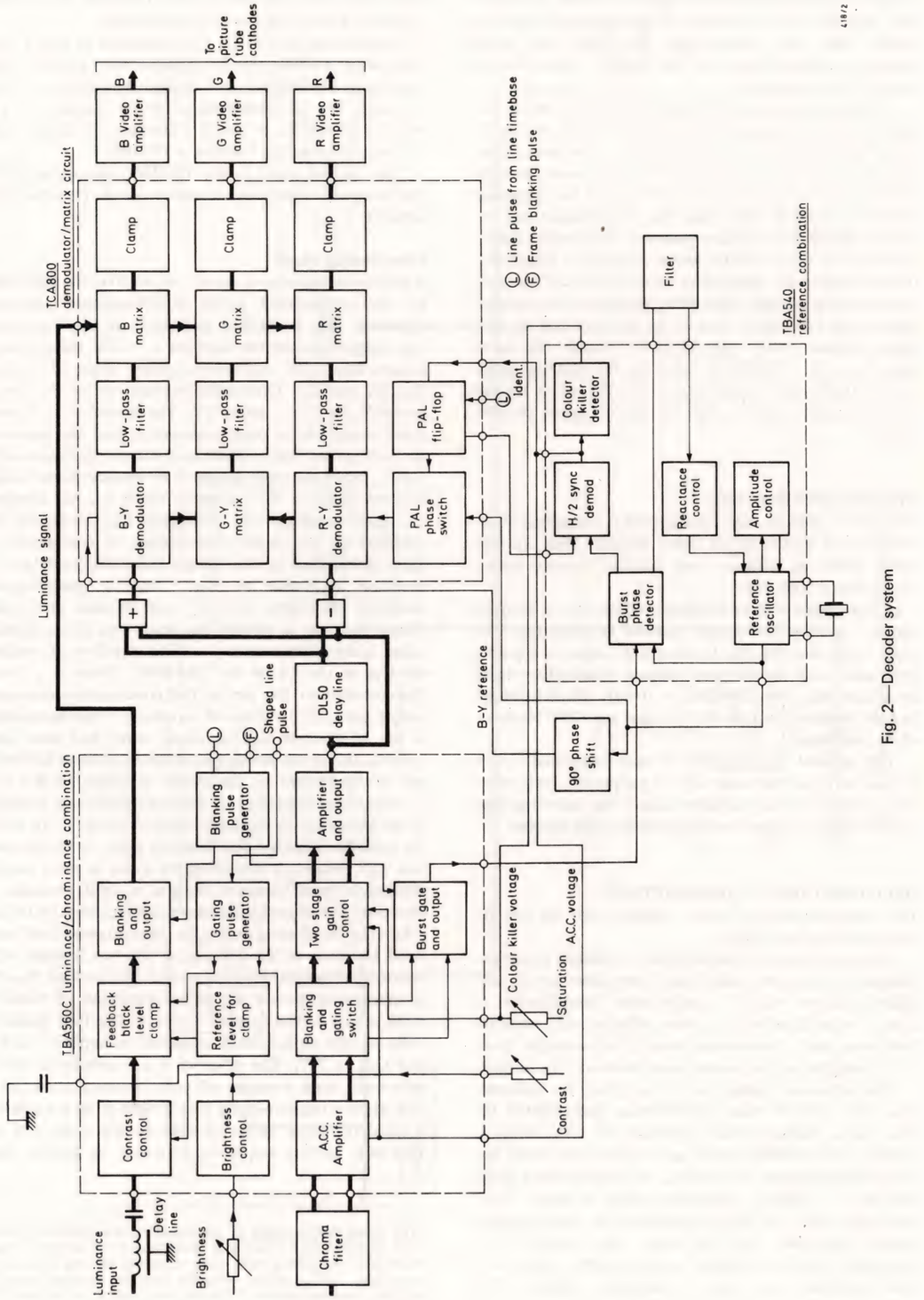

Fig. 2—Decoder system

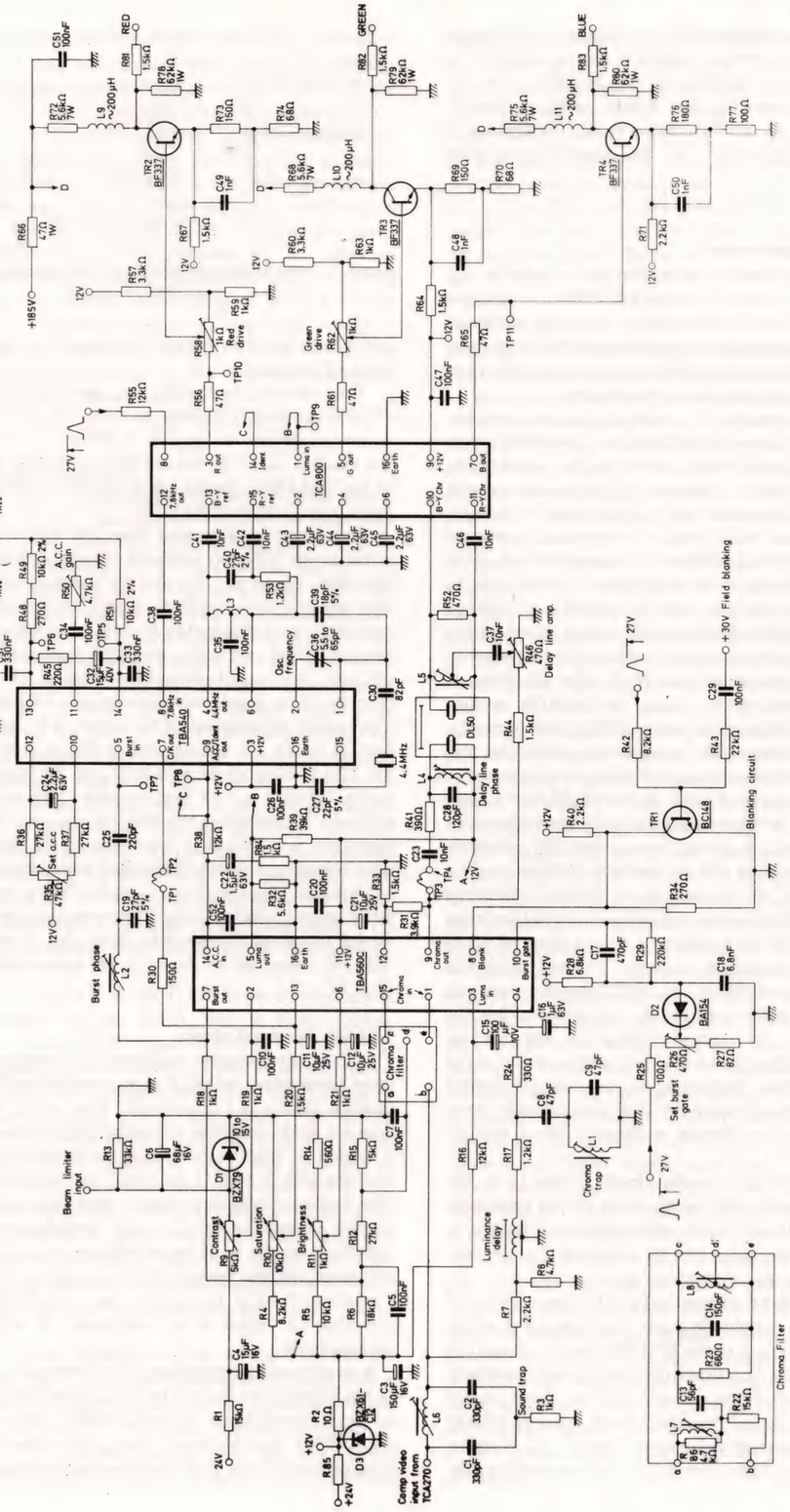

Fig. 3—Complete decoder circuit (For component list, see Appendix)

1·5V peak-to-peak. Because TR_1 is saturated for the field flyback period, its output waveform is not suitable for triggering the PAL flip-flop in the TCA800. For this purpose, a positive-going line flyback pulse is directly applied to pin 8 of the TCA800, via R_{55}. Triggering of the PAL flip-flop occurs on the negative-going edge of this pulse.

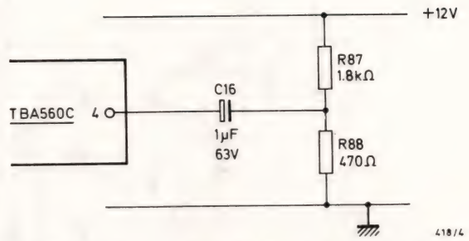

Fig. 4—Circuit to increase tolerated level of power supply hum from 5mV to 40mV

TBA560C peripheral circuit

The picture brightness is controlled by a variable d.c. potential applied to pin 6 of the TBA560C. A variation between 0·7V and 1·7V will cover the entire range of black-level variation (on pin 5) from 0V to 3V. This is more than is needed in practice, and the range of the control can be restricted to suit particular requirements.

During the operation of a correctly adjusted receiver, variations in the transmitted picture can occasionally cause the safe limit of mean beam current in the picture tube (typically 1·5mA total) to be exceeded. Such excesses should be dealt with by a reduction in picture contrast to maintain the correct picture black-level. A convenient source of beam current information occurs at the earthy end of the e.h.t. supply network. The mean beam current can be sampled directly here and used to control the contrast level in the TBA560C. Diode D_1 is forward-biased during normal operation by a current of about 1·5mA supplied via the contrast control network R_1 R_9. For all values of mean beam current below 1·5mA, the diode D_1 remains conducting and the contrast control functions normally. Above 1·5mA, however, D_1 becomes non-conducting and the bottom end of the contrast control is driven negatively, thus reducing the contrast level. No threshold level adjustment is required, and provided that the current source for the contrast network is derived from at least 20V, adequate loop gain is achieved. A voltage regulator diode is used for D_1 with 10 to 15V reverse breakdown voltage, to limit the negative potential in the event of serious overload and thus protect the IC and the capacitor C_6. The value of C_6 is chosen as a compromise between a small parabolic variation in contrast caused by field frequency ripple in the e.h.t. circuit and an adequately fast reaction time for the control loop. The supply voltage for the contrast control network should be sufficiently ripple-free to avoid the need for further decoupling in the contrast control network, which would make the loop time-constant complicated, possibly introducing oscillatory effects into its operation.

The presence of 12V supply ripple at pin 11 of the TBA560C may cause undesirable ripple on the luminance output at pin 5. Power supply ripple should be limited to 5mV, but a greater value can be tolerated if additional resistors R_{87}, R_{88} are connected as shown in Fig. 4.

A luminance signal of nominally 1·7V black level and 1V black-to-white amplitude is produced on pin 5 and is directly coupled to pin 1 of the TCA800. The d.c. potentials controlling contrast and saturation are applied independently to pins 2 and 13 respectively. For any given setting of the saturation control R_{10}, the chroma signal amplitude will track adjustment of the contrast control R_9. Also for any given setting of these controls the contrast and chroma levels track together during operation of the beam current limiting function.

The network R_6 R_{12} R_{15} sets the d.c. working point of the burst amplifying channel in the TBA560C. The a.c.c. potential applied to pin 14 is filtered by the network R_{38} C_{52} R_{84} C_{22}. The colour killer potential from pin 7 of the TBA540 is applied via R_{30} to the saturation control point, pin 13 of the TBA560C.

The colour burst output from pin 7 of the TBA560C is fed to the TBA540 reference combination via the low-pass filter circuit L_2, C_{19} and the coupling capacitor C_{25}. This circuit is included for two main reasons, the principal one being to compensate for residual phase shifts in the decoder. These amount to about 15° lagging with a spread of ±10°, so that a leading phase shift of 15° is required from this filter circuit, with an adequate adjustment range. The second requirement of the circuit is to give a voltage gain of about 1·5 because the optimum burst output of the TBA560C is 1V peak-to-peak and the optimum input to the TBA540 is 1·5V peak-to-peak. This can be simply achieved by operating the filter circuit near its resonant frequency and choosing a suitable Q, to give a circuit with voltage gain and a reasonably wide adjustment range as required. The circuit has a phase shift at resonance of 90° (lagging) which is simply compensated by a suitable choice of output connections from pins 4 and 6 of the TBA540; these are as shown in the main circuit diagram (Fig. 3).

TBA540 peripheral circuit

The TBA540 reference oscillator IC receives its colour burst input signal on pin 5 at an amplitude of 1·5V peak-to-peak (under a.c.c. control). The a.p.c. loop phase detector loads and filter are connected to pins 13 and 14. A crystal of 20pF nominal load capacitance is connected between pins 1 and 15 to form the reference oscillator. The oscillator reference output waveform from pin 4 is applied to transformer L_3 which produces an antiphase waveform on pin 6. These waveforms are applied via the 90° phase shifting network R_{53} C_{40} and via d.c. blocking capacitors C_{41} C_{42} to pins 13 and 15 of the TCA800 demodulator circuit at an amplitude of about 700mV peak-to-peak.

A synchronously-generated a.c.c. potential is produced at pin 9 and is fed via resistor R_{38} to the TBA560C. With no burst signal input to the TBA540, the potential on pin 9 (TP8) is set by R_{35} to +4V. When the burst signal is applied, and if the PAL flip-flop phase in the TCA800 is

correct, this potential will drop until a.c.c. control is established (1·5V peak-to-peak burst signal amplitude). This condition corresponds to about +1V on pin 9 of the TBA540. If the flip-flop phase is incorrect the potential on pin 9 would rise to +10V, passing a positive potential to the flip-flop ident control point, pin 14 of the TCA800. The PAL flip-flop in the TCA800 would stop, thus removing the switching waveform from the a.c.c. synchronous detector in the TBA540 (pin 8). As a result the a.c.c. potential on pin 9 would drop towards 0V thus allowing the flip-flop to start up again. The colour killer switching output from the TBA540 is produced at pin 7 from the collector of a transistor which is saturated for incorrect ident (giving a voltage of +250mV) and is off for the correct ident; the switching of this transistor occurs as the voltage on pin 9 passes +2·5V.

TCA800 peripheral circuit

The input signal requirements of the TCA800 follow closely those of the TBA990 and TBA530. A luminance input signal from the TBA560C is applied to pin 1. Nominal blanking and black input levels are at 1·5 and 1·7V respectively, and a black-to-white amplitude of 1V peak-to-peak that is required for maximum contrast is adjusted by the contrast control function of the TBA560C. The brightness control of the TBA560C adjusts the d.c. level of the picture information relative to the fixed d.c. potential that is maintained during the blanking interval for pin 1 of the TCA800. This blanking potential may be set to 1·5V either by a potential divider at the luminance output of the TBA560C, when the device is set to blank to zero volts, or by using a different blanking pulse input to the TBA560C so that it will itself produce a luminance signal blanked to 1·5V. In the latter case, negative-going blanking pulses of nominally 2·5V peak-to-peak have to be a.c. coupled to pin 8 of the TBA560C, otherwise a pulse of not greater than −1V may be d.c. coupled, with the negative excursion at zero volts.

On pins 2, 4, and 6 of the TCA800 are connected the clamp capacitors for the R, G, and B video outputs respectively. These 2·2μF capacitors, C_{43}, C_{44}, and C_{45}, store the blanking potential derived from the blanked video waveforms at the RGB outputs of the TCA800. The clamp capacitors are charged via a gate circuit, driven by internally derived pulses that are of shorter duration than the line flyback pulses applied at pin 8. The potentials at each of the clamp capacitors are compared within the TCA800 to a single stable reference potential to effect the clamping of the RGB output signals. In this way any differential drifts or offsets of the RGB output potentials are reduced to a minimum. Electrolytic capacitors of 2·2μF from the 015 series are suitable for use as the clamp capacitors.

The R, G, and B video outputs of the TCA800 are produced at pins 3, 5, and 7 respectively. Each has a blanking level clamped at 2V with a blanking-to-white capability of typically 7·5V. The blanking potential is determined by a potential divider from the 12V supply within the TCA800, and so will track with supply voltage variations. A luminance amplification of 5 times results in a black-to-white amplitude of 5V and a black level at 3V, assuming the luminance input conditions that have been specified for pin 1. The −3dB bandwidth of the luminance amplifiers from pin 1 to the RGB outputs is greater than 5MHz. The maximum difference between the clamped blanking levels of any two of the RGB outputs is less than 50mV, and the differential drift over a 40degC temperature rise is less than 25mV. Output signals that are supplied from internal emitter followers are suitable for directly driving video output transistors. Flashover protection and short-circuit protection are provided at the RGB outputs. Flashover protection is provided by internal diodes which, together with external series resistors, limit dissipation within the TCA800 should flashover occur.

A positive-going line pulse is required at pin 8, applied via an external series resistor. The pulse is used within the TCA800 to trigger the PAL flip-flop and to gate the feedback clamp potentials from the video output waveforms. For the latter function, in order to avoid transients at the extremes of the blanking interval on incoming luminance signals, a somewhat narrower pulse is produced internally. By using a threshold of 12·5V, and a pulse that is d.c. coupled from a winding of the line output transformer through a resistor to pin 8, a current waveform may be produced there of the required amplitude and of less width. In practice a pulse from the line transformer that is greater in amplitude than 12·5V must be used, and this may be perhaps 18V or 27V peak-to-peak, dependent upon the variation of pulse amplitude expected with beam current and supply mains changes. The series resistor is then proportioned to give a minimum current during the gating interval between 0·3 and 0·6mA. A resistor of between 12kΩ and 18kΩ is appropriate for a 27V line pulse.

On no account, during any expected operational situation in the receiver, should the clamp pulse waveform deteriorate to such an extent that the clamping functions in the TCA800 are inoperative; otherwise, shifts in d.c. level of the output signals could occur.

The positive 12V supply is applied at pin 9. This supply should not be allowed to exceed 13·2V under normal conditions. All signals and control potentials have a linear dependence upon voltage. In any given receiver design this may be restricted by considerations of tracking between power supply variations and picture levels. The minimum supply voltage is 10·8V, and the typical supply current is 65mA. Pins 10 and 11 are the B-Y and R-Y chrominance signal inputs respectively. The input resistance of each is typically 800Ω, and the input capacitance is 10pF. The B-Y signal required is typically 130mV peak-to-peak and the R-Y signal 170mV peak-to-peak. A d.c. blocking capacitor of 10nF must be included in series with either pin 10 or pin 11. Pins 13 and 15 are the B-Y and R-Y subcarrier reference inputs. Signals of about 1V peak-to-peak are required at each input, and the input impedances are 5kΩ in parallel with 5pF. Adequate switching of the demodulators is maintained with peak-to-peak reference input amplitudes down to 500mV. The B-Y reference is derived from pin 4 of the TBA540. At pin 4 the oscillator is in B-Y phase as the burst phase shift circuit produces a 90° phase shift.

At pin 12, an internal emitter follower provides an output voltage of 3·5V peak-to-peak at a frequency of 7·8kHz. No external load resistor is required. This pin is a.c. coupled by a 100nF capacitor to pin 8 of the TBA540.

The PAL flip-flop is stopped, for identification purposes, when the voltage on pin 14 rises above 6·5V. The threshold is internally defined and has a proportional behaviour with the 12V supply rail. The threshold level of 6·5V is chosen to match the output characteristic from pin 9 of the TBA540, and has a sufficiently high safety margin above the zero colour burst level of 4V to eliminate spurious identifying. However, because it is advantageous not to restrict the device to tied use, a modified ident control (flip-flop) drive input circuit is employed on the chip to permit alternative operation with a typical discrete-component reference and ident circuit; for example, where a narrow-band amplifier develops a 7·8kHz flip-flop drive waveform.

VIDEO OUTPUT STAGES

To minimise the fixed spreads and operational drifts in the d.c. levels of the picture tube drive signals, the gain figures for video output stages not having overall feedback should be as low as possible. The large drive signals available from the TCA800 enable a maximum drive amplitude of 100V black-to-white to be achieved with a stage gain of only 20 times; therefore the contribution that the video output stages make toward picture drifts can be kept small.

A highly desirable economy in a receiver is the elimination of d.c. level adjustments in the RGB circuits. This can be done if the fixed tolerances in the d.c. levels of the drive signals are sufficiently small to be adequately covered by the picture tube a_1 adjustments. It is believed that, if the differential fixed d.c. level tolerances on the drive signals do not exceed $\pm$5V peak-to-peak, all recommended picture tubes can be set up by the a_1 adjustments alone to have acceptable grey scales.

During operation, simple video stages will contribute towards unwanted picture variations that are due mainly to d.c. drifts caused by heating of the output transistors, but these drifts can be limited in extent by a suitable choice of heat fin performance.

A detailed study has been made of output stage drift performance, and this will be summarised, dividing the effects into two main categories: fixed set-to-set production tolerances, and variations during operation, each being subdivided into common-mode and differential varieties.

D.C. level spreads due to component tolerances

The simple video stage of Fig. 5 can be taken as an example for study. To avoid serious variation of the output black level during gain adjustment (white point setting) a constant black level type of gain control is used. Its range of gain adjustment is from 0·6 to 1·3 times, and for the purpose of analysis it is set to 80% of maximum gain. A split collector load is employed, R_7 R_9, as an example of reducing the voltage supplied to the transistor to minimise power dissipation.

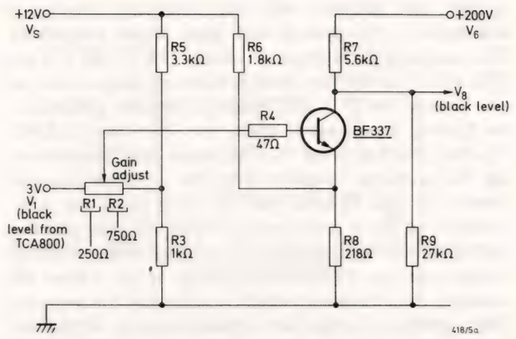

Fig. 5—Basic video stage

Common d.c. level spreads

The three stages will have common supply voltages, V_5 and V_6, and the TCA800 will feed practically equal black level potentials, V_1, to each stage. Thus these voltages alone determine the common-mode component of spread in the output trio. These spreads can be considered as simple fixed tolerances which can, in principle, be accommodated in the range of the receiver a_1 adjustments or brightness control, or both.

Differential d.c. spreads

The differential spreads are caused chiefly by the differences between resistor and transistor tolerances in the three output stages.

A computer analysis was carried out on the typical circuit of Fig. 5, to study the extent and distribution of the d.c. level spreads and also to determine the relative importance of given tolerances in the various parameters. For the analysis the following assumptions were made:

a) A Gaussian distribution of all the resistor values in the range $\pm$5%.
b) Transistor parameters:
   Leakage current I_{CBO}, 5 to 20μA
   Current gain, 22 to 80
   Base-emitter voltage V_{BE}, nominal curve $\pm$100mV.
c) Voltages V_5 and V_6 fixed (these are responsible for common-mode spreads only).
d) Voltage V_1 fixed.

The result of 3000 cases is shown in Fig. 6, where the vertical left-hand scale represents the black level potential of the output signal (V_8), computer-derived by a Monte Carlo analysis, and the column of figures on the right-hand side gives the number of cases found at each level. All but a few cases lie within a range of $\pm$5V about the mode of 146·5V. Only a small proportion of picture tubes may produce a noticeably degraded grey scale when subjected to differential spreads in gun cathode potentials sensibly in excess of $\pm$5V. Because the probability of the combination in a receiver of a limit picture tube gun and an output

DISTRIBUTION OF PERFORMANCE PARAMETER V8 FOR 3000 CASES TESTED

```
141.279                                                                                                    1
141.513      *                                                                                             2
141.746      *                                                                                             2
141.979                                                                                                    1
142.213      **                                                                                            6
142.448      **                                                                                            5
142.679      ***                                                                                          10
142.913      *****                                                                                        17
143.146      ********                                                                                     26
143.379      *********                                                                                    30
143.613      **********                                                                                   32
143.846      ****************                                                                             53
144.079      ****************                                                                             54
144.313      **********************                                                                       70
144.546      **********************                                                                       72
144.779      ****************************                                                                 90
145.013      ********************************                                                             97
145.246      **************************************                                                      119
145.479      ****************************************                                                    128
145.713      ******************************************                                                  136
145.946      ********************************************                                                142
146.180      **********************************************                                              157
146.413      ********************************************                                                146
146.646      ************************************************************                                180
146.880      **********************************************                                              153
147.113      ************************************************                                            159
147.386      **********************************************                                              150
147.580      ******************************************                                                  140
147.813      ********************************************                                                146
148.045      ****************************************                                                    123
148.280      ********************************                                                          104
148.513      ******************************                                                             93
148.746      ******************************                                                             90
148.980      **********************                                                                     72
149.213      ******************                                                                         59
149.446      ************                                                                               41
149.679      *********                                                                                  31
149.913      *******                                                                                    24
150.146      ****                                                                                       13
150.380      ***                                                                                         9
150.613      ***                                                                                         9
150.846      *                                                                                           4
151.080                                                                                                  1
151.313                                                                                                  1
151.546                                                                                                  1
151.780                                                                                                  0
152.013                                                                                                  0
152.246                                                                                                  0
152.480                                                                                                  0
152.713                                                                                                  1
```

STATISTICAL PARAMETER VARIATIONS FOR 3000 CIRCUITS TESTED:

PARAMETER	MINIMUM	MEAN	MAXIMUM	NOMINAL	STD. DEV.
V8	141.3	146.6	152.7	146.5	1.661

Fig. 6—Distribution of performance parameter V_8 for 3000 cases tested

stage at the limit in the opposite direction is rather low, the overall incidence of troublesome grey scale adjustment is likely to be small.

If a narrower spread in d.c. level from the output stages is required, certain components of closer tolerance could be used. The effect on the d.c. level of a ±5% variation on each resistor is as shown in Table 1.

TABLE 1

Effect of Resistor Tolerances on D.C. Output Level

R±5%	V_8 (volt)
R_1 }	negligible
R_2 }	
R_3	∓0·3
R_4	±0·003
R_5	±0·28
R_6	∓1·1
R_7	∓2·2
R_8	±1·9
R_9	±1·2

A tightening of tolerances for R_7 and R_8 would therefore yield the best advantage.

In a case where accurate adjustment of d.c. level is deemed necessary a portion of R_6 could be made variable, its value having small influence upon the stage gain.

Drifts in d.c. levels due to operational variations

Common-mode variations

Any variations in h.t. or l.t. supplies in a receiver will produce common-mode variations in the d.c. levels of the drive signals supplied to the picture tube. In the circuit of Fig. 5, these are potentials V_1, V_5, and V_6. The design of the TCA800 is such that V_1 has proportional tracking with the 12V supply so that V_1, V_{R3}, and V_{R8} all track together, thus producing the minimum influence upon the output signal black level potential. The effect of variations of V_6 is determined by the ratio of R_7 and R_9.

However, whether the supply potentials of a receiver are stabilised or not, there will occur variations of output signal black level caused by temperature effects in the video transistors. This is due chiefly to the dependence of V_{BE} upon temperature (approximately —2mV/degC) which with a stage gain of 20 times affects the output d.c. level at a rate of −40mV/degC. The design of the TCA800 includes a similar temperature dependence of the d.c. levels of the output signals to give useful partial compensation against the effects in the video output transistors. This type of compensation, however, is limited because the integrated circuit chip cannot be in close thermal contact with the video transistors.

Variations in the luminance content of the transmitted signal will change the power dissipation in the output stages and thereby cause common-mode variations in the output signal d.c. levels. The effect is estimated by the following example.

Video output stage characteristics
(circuit of Fig. 5)

R_L	4·9kΩ
$V_{h.t.\ (eff)}$	165V
V_{black}	145V
V_{white}	45V
$V_{mid-grey}$	82·5V (worst case)
$V_{blanking}$	165V (cut off)
Blanking interval	15%
$R_{th(j-amb)}$	70degC/W

The three chlef cases of power dissipation in the video transistor are as follows:

$$P_{black} = 145 \times \frac{165-145}{4{\cdot}9} \times \frac{85}{100} = 0{\cdot}49W$$

$$P_{white} = 45 \times \frac{165-45}{4{\cdot}9} \times \frac{85}{100} = 0{\cdot}94W$$

$$P_{mid-grey} = \frac{165^2}{4 \times 4{\cdot}9} \times \frac{85}{100} = 1{\cdot}18W$$

Thus:

	Black	White	Mid-grey
Junction temperature rise above ambient (degC)	34	66	82
ΔV_{BE}(mV)	−68	−132	−166
ΔV_{output}(G = 20) (V)	−1·36	−2·64	−3·32

The worst variation in d.c. level during viewing is therefore 1·96V; that is, about 2% of the maximum black-to-white output.

From receiver switch-on, a warming-up drift will occur as the TCA800 chip and the video transistors rise from ambient to their working temperatures. Some compensation will occur between the integrated circuit and the video stages, but their temperature excursions are different as are their thermal time-constants. With a video stage of the type shown in Fig. 5, calculations indicate that when switching on from an ambient of 20°C to a running condition where a mid-grey (highest transistor dissipation) raster is displayed, the change in output signal d.c. level is around −4V. Measurements on a practical receiver have indicated a somewhat smaller drift.

It is noteworthy that although, in essence, the above effects are common-mode operational variations, their influence on the picture will not necessarily be a pure brightness variation. This is due to the tolerances in the slopes of the picture tube gun assemblies and phosphor sensitivities. These can result in an overall tolerance in effective gun sensitivity between limit guns of some ±13%. Therefore for a given common-mode variation in the d.c. level of the drive signals there may be in the worst case some 13% of that variation appearing as a differential change in colour of the picture. This is clearly a second-order effect and has not been found to be objectionable in practical receivers.

Differential operational variations

Given effective d.c. level stability of the RGB signals supplied by the TCA800, the chief cause of differential d.c. level variations in the video stage output signals is the varying power dissipation in each of the three stages due

to changing picture colour modulation. A comprehensive analysis of these effects upon the picture would be complicated by the effect of tolerances in picture tube gun and phosphor sensitivities. However, it is useful to consider what the worst possible drifts might be in the case of a nominal picture tube.

A nominal picture tube having equal gun and nominal phosphor sensitivities has RGB drive signal ratios of typically 1·0:0·91:0·84 respectively for illuminant 'D'. At black, each nominal output stage will have the same power dissipation, but with any other signal the dissipations are most likely to be different. The chief causes of d.c. drift in the transistors are the dependence of V_{BE} (−2mV/degC) and β (0·48/degC) upon temperature. Calculations applying these variables to a typical output stage as already defined give the following results:

	peak-to-peak differential variations at outputs
a) Due to a change in all the stages from black level to a mid-grey* field.	0·276V
b) Due to a pure coloured field at 'mid-grey' level resulting in one stage operating at maximum power dissipation while the other two remain at black level.	2·76V
c) That due to (b) but including the effect of the high dissipation stage having a heat fin performance 5% lower than the other two.	2·83V
d) Due to the worst combination of (b) and (c) together with a 10% lower collector load resistance in the stage operating at maximum power dissipation.	3·3V

The result for (d) indicates the worst likely drop in d.c. level of a stage supplying drive for a single-coloured saturated field under an adverse combination of circumstances. Assuming that a sustained red field had just finished, therefore, the picture could have an excess of red for a short time afterwards. Because the effect of a sustained saturated coloured field upon the human eye is to give afterwards a bias in favour of the complementary colour, some subjective compensation probably occurs in certain cases.

ALIGNMENT PROCEDURE

The alignment procedure is described below in some detail for clarity. Many of the procedures are intended to give a simple indication suitable for a production test.

1) Check that the l.t. supply lies within 12V±5% or set it to this level in the case of an adjustable regulation.

Luminance channel adjustments

2) Connect TP1 to earth to kill the chroma channel, so that the output signals from the TBA560 are zero amplitude.

*Output level, 82·5V, giving the highest power dissipation in the transistors.

3) Reduce the contrast to zero using the contrast control R_9. The brightness control should then be adjusted to give a d.c. level during scan of 150V, at the collectors of the three video output transistors. This potential may be measured using either an oscilloscope or an Avometer. In the latter case, taking account of the positive excursions of the blanking waveforms, the measured value should be 154V. (150V is the nominal black level voltage at the collectors of the video output transistors for the circuit of Fig. 3).

4) The cut-off controls used for adjusting the voltages applied to the a_1 electrodes of the CRT must now be adjusted for raster cut-off on each gun.

5) Apply a 'grey scale' signal from a pattern generator and adjust the contrast and brightness controls to obtain a suitable picture.

6) Adjust variable resistors R_{58}, R_{62} to obtain the correct white point of the display. As these controls are of the constant black level type there will be a minimum of interaction with the cut-off (a_1) controls. In a few cases, variations in CRT drive characteristics between guns will make a small readjustment of cut-off controls necessary to ensure a uniform grey scale.

7) L_1 should be adjusted to minimise the residual sub-carrier content in the video drive to pin 1 of the TCA800, by observing the luminance signal at TP9 when a colour bar signal, for example, is applied from a pattern generator.

Chrominance channel adjustments

8) The following adjustments to the chrominance circuits should be carried out with a colour bar signal from a pattern generator. Adjust the chrominance bandpass filter at the input of the decoder for optimum response. Remove the short-circuit between TP1 and earth, and remove the link between TP1 and TP2. Adjust the saturation control to give a suitable picture on the screen. With the flywheel system correctly phased, check that the gating pulse for the colour burst is correctly timed by observing the gated burst at TP7. Adjust the timing of the burst gating pulse by means of R_{26} if necessary. The burst should be centrally situated in the gating interval.

9) Adjust the reference oscillator TBA540 as follows. Short-circuit TP5 to TP6 in order to disable the burst phase detector. The starting point of the a.c.c. voltage (corresponding to reception of zero chrominance signal) can now be adjusted by observing the voltage at TP8. This should be set to 4·0V by means of R_{35}.

10) The reference oscillator frequency may be adjusted by means of C_{36} until the rolling of the colours is almost brought to a standstill; that is, the regenerated sub-carrier frequency is within a few hertz of the transmitted subcarrier frequency.

11) Remove the short-circuit between TP5 and TP6. The reference oscillator should lock to the colour burst.

12) Adjust the a.c.c. gain control R_{50} until the burst amplitude at TP7 is 1·5V peak-to-peak.

13) The adjustment of subcarrier phase and delay line balance can be achieved either by the use of a pattern generator such as the Philips PM5508 or by the use of a standard colour bar signal and an oscilloscope as described in procedures 14 to 19.

With the PM5508 pattern generator, the adjustment procedure is as follows. Select the PHASE pattern and adjust the coil L_2 until the colour of each bar is the same in both parts of the screen. Select the DELAY pattern and adjust R_{46} and L_4 until the 'Hanover bars' visible are reduced to zero. Adjustments of the delay line input and output coils L_4 and L_5 both affect the phase delay. However, the output coil should be pre-adjusted during manufacture to its nominal inductance of 8·9μH, and delay (phase balance) adjustments are made with the input coil L_4, which has twice the effect of the output coil L_5 on the delay. By this means most of the delay spreads can be adjusted out within the permitted −19 to +36% variation of input coil inductance, without any serious reduction of the frequency response of the delayed signal path. If the worst-case spreads of delay are encountered, so that it is not possible to achieve phase balance with the input coil L_4, then the output coil L_5 may be adjusted. The total variation possible with −19 to +36% inductance range in both coils is sufficient to take up all spreads with minimum reduction of the frequency response, the bandwidth remaining greater than 1·8MHz. After adjustment of the delay line phase and amplitude balance, select the PHASE pattern again and check the subcarrier phase adjustment.

14) The alternative procedure, with a standard colour bar signal and an oscilloscope, is as follows: the oscilloscope is connected to TP10 (Red output of the TCA800) and triggered by line pulses in such a way that two adjacent lines are superimposed.

15) Open-circuit TP3 and TP4. This effectively isolates the delay line and transforms the decoder to simple PAL operation, which makes subcarrier phase errors obvious as line-to-line differences. To correct the phase of the R-Y subcarrier, the burst phase shift coil L_2 is adjusted until the double pictures seen on the oscilloscope are made to coincide.

16) Connect the oscilloscope to TP11 and check that the line-by-line difference in the Blue output of the TCA800 (at TP11) is reduced to zero, or nearly so. Thus the phase adjustment of the reference subcarriers is made by a null method, which gives a very clear indication of error.

17) The phase adjustment of the DL50 delay line can now be carried out. Replace the connection between TP3 and TP4, and continue to observe the Blue colour difference output at TP11 or the Red output at TP10. Errors in phase balance of the delay line will be seen as line-by-line differences in the colour bars with large R-Y content, namely the cyan, green, magenta, and red bars. The phase adjustment should be performed as in procedure 13; that is, beginning with the delay line input coil L_4, until the double pictures viewed on the oscilloscope are made to coincide.

18) Amplitude balance errors in the delay line, which will result in the presence of B-Y chrominance signal in the R-Y chrominance input to the TCA800 and *vice versa*, will not give rise to any line-by-line disturbances in the colour difference outputs, as the phases of the reference subcarrier signals have been precisely adjusted to procedures 15 and 16. To obtain a line-by-line error which will indicate any amplitude unbalance of the delay line, it is thus necessary to shift the overall phase of the reference subcarrier signals from the nominal position, preferably by 90°. Connect a 1nF capacitor across L_2 and C_{25} (this will give a phase error greater than 30°) and adjust R_{46} to reduce the line-by-line differences to zero, viewing the Blue signal at TP11 or the Red signal at TP10, as before.

19) Remove the 1nF shorting capacitor and reconnect the link between TP1 and TP2 to restore correct operation of the colour killer.

APPENDIX

Components List

Fixed resistors

The Mullard CR25 (±5%) series can be used for all fixed resistors except the following:

R_{49} and R_{51}—Mullard MR25 series (±2%)
R_{68}, R_{72}, R_{75}, R_{85}—Vitrohm 7W (±5%)
R_{66}, R_{78}, R_{79}, R_{80}—Dubilier BTA (carbon) series 1W (±5%)

Adjustable resistors

Variable resistors

R_9, R_{10}, R_{11}—Morganite 30N series

Preset resistors

R_{26}, R_{35}, R_{46}, R_{50}, R_{58}, R_{62}—RS Components miniature presets

Inductors

Winding details for the coils, except L_4, L_5, and those in the video output stages, are given in Table 2.

Capacitors

Circuit Ref.	*Value*	*Mullard Type No.*
C_1	330pF	C333CH/C330E
C_2	330pF	C333CH/C330E
C_3	150μF 16V	016 15151
C_4	15μF 16V	015 15159
C_5	100nF	C280AE/P100K
C_6	68μF 16V	016 15689
C_7	100nF	C280AE/P100K
C_8	47pF	C333CC/C47E
C_9	47pF	C333CC/C47E
C_{10}	100nF	C280AE/P100K
C_{11}	10μF 25V	015 16109
C_{12}	10μF 25V	015 16109
C_{13}	56pF	C333CC/C56E
C_{14}	150pF	C333CC/C150E
C_{15}	100μF 10V	016 14101
C_{16}	1μF 63V	015 18108
C_{17}	470pF	630 02471
C_{18}	6·8nF	
C_{19}	27pF	C333CC/C27E
C_{20}	100nF	C280AE/P100K
C_{21}	10μF 25V	015 16109
C_{22}	1·5μF 63V	015 90001
C_{23}	10nF	C280AE/P10K
C_{24}	2·2μF 63V	015 18228
C_{25}	220pF	C333CH/C220E
C_{26}	100nF	C280AE/P100K
C_{27}	22pF	C333CC/C22E
C_{28}	120pF	C333CC/C120E
C_{29}	100nF	C280AE/P100K
C_{30}	82pF	C333CC/C82E
C_{31}	330nF	C280AE/A330K
C_{32}	15μF 40V	015 17159
C_{33}	330nF	C280AE/A330K
C_{34}	100nF	C280AE/P100K
C_{35}	100nF	C280AE/P100K
C_{36}	5·5 to 65pF	808 01001
C_{37}	10nF	C280AE/P10K
C_{38}	100nF	C280AE/P100K
C_{39}	18pF	C333CB/C18E
C_{40}	27pF	C333CC/C27E
C_{41}	10nF	C280AE/P10K
C_{42}	10nF	C280AE/P10K
C_{43}	2·2μF 63V	015 18228
C_{44}	2·2μF 63V	015 18228
C_{45}	2·2μF 63V	015 18228
C_{46}	10nF	C280AE/P10K
C_{47}	100nF	C280AE/P100K
C_{48}	1nF	630 02102
C_{49}	1nF	630 02102
C_{50}	1nF	630 02102
C_{51}	100nF	C280AE/P100K
C_{52}	100nF	C280AE/P100K

Transistors and Diodes

TR_1	BC148
TR_2	BF337
TR_3	BF337
TR_4	BF337
D_1	BZX79 (10 to 15V)
D_2	BA154
D_3	BZX61–C12

TABLE 2

Coil Winding Details

Coil number	Former	Winding	Turns	Wire	Core
L_1	EIH P1011/1	Wavewound 6·4mm length	70	0·1mm en.cu.	NEOSID 500×6mm
L_2	EIH P1011/1	Wavewound 6·4mm length	70	0·1mm en.cu.	NEOSID 500×6mm
L_3	NEOSID 4060 (F14)	Scramble	18+18	0·1mm en.cu. bifilar wire	NEOSID 4060
L_4	Mullard delay line coil AT4044/00				
L_5	Mullard delay line coil AT4044/01				
L_6	EIH P1011/1	Single layer	30	0·1mm en.cu.	NEOSID 500×6mm
L_7	EIH P1011/1	Wavewound 6·4mm length	80	0·1mm en.cu.	NEOSID 500×6mm
L_8	EIH P1011/1	Single layer	20+20 bifilar	0·1mm en.cu.	NEOSID 500×6mm

LP1400 stereo decoder module

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UDC 621.396.621: 621.376.33[534.76]

Stereo broadcasting is discussed, time multiplex and frequency multiplex decoding systems are described, and the performance of the two systems compared. The LP1400 stereo decoder module using the frequency multiplex system is described and details of performance are given. Applications of the LP1400, and details of an f.m. tuner which uses modules, are also included.

INTRODUCTION

Stereophonic broadcasting has grown from some of the early BBC sound broadcasts, with each channel transmitted by separate medium-wave stations, to the high-quality v.h.f. stereophonic transmissions of the present day. The early methods of transmission suffered from disadvantages of:

duplication of transmitting and receiving apparatus,

restriction to hearing half (one channel) of the original programme if only one transmission could be received.

In 1961, the Zenith-GE stereo system (now known internationally as the pilot-tone system) was chosen by the U.S. National Stereophonic Radio Committee. Frequency-modulated (f.m.) stereophonic broadcasts began in the same year, requiring only one transmitter and one receiver operating on a single frequency.

PILOT-TONE SYSTEM

In the pilot-tone system, the transmitter modulation consists of three components (see Fig. 1), a sum signal (L+R)/2, a difference signal (L−R)/2, and a pilot-tone. The combination of these components is termed 'composite', or 'multiplex'. 'L' is the left-channel signal and 'R' the right-channel signal. The instantaneous deviation of the transmitter carrier is:

$$\left[0{\cdot}9\left(\frac{L+R}{2}+\frac{L-R}{2}\sin 2\omega t\right)+0{\cdot}1\sin\omega t\right]\times 75\text{kHz}$$

where the expression inside the inner brackets represents the multiplex signal (0·1sinωt is the 19kHz pilot-tone).

Sum signal

The sum signal (L+R)/2 consists of left- and right-channel audio frequencies. It is a compatible signal to which monophonic and stereophonic receivers respond.

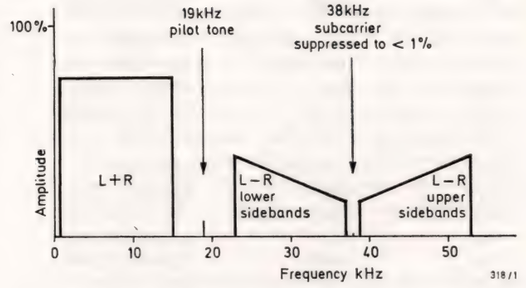

Fig. 1—Spectrum of multiplex modulation signal

Difference signal

The difference signal (L−R)/2 is transmitted as two sidebands, extending from 23kHz to 53kHz, about a suppressed carrier frequency of 38kHz. The difference signal is used to separate the left- and right-channel signals.

Pilot-tone

The pilot-tone (0·1sinωt) is a 19kHz sinewave, phase-locked to the 38kHz subcarrier. It is a constant-amplitude signal, maintained at 10% of the full carrier deviation. The pilot-tone is used in the recovery of the difference signal from the sidebands of the suppressed carrier.

Pre-emphasis

Pre-emphasis is applied to left- and right-channel signals. The time-constant of the pre-emphasis is 50μs for monophonic and stereophonic transmissions in most countries, including Britain. Exceptions are America and Japan, who use 75μs pre-emphasis in their transmissions.

High-frequency audio signals are boosted in amplitude by the pre-emphasis, requiring de-emphasis in the receiver. In the de-emphasis, much of the audible receiver noise is eliminated.

To extract left- and right-channel signals from the multiplex transmissions, a decoding system is necessary. Two methods of decoding are described here: the time multiplex system and the frequency multiplex system.

This article is based on work done by H. Q. N. Davies while in the Quality Laboratory of Electronic Assemblies Division, Mullard, Mitcham.

TIME MULTIPLEX DECODING SYSTEM

In the time multiplex decoding system, the complete composite stereo signal is switched between left and right channels at the subcarrier frequency of 38kHz. Provided that the phase of the subcarrier is correct, the left-channel signal will be present at the left-channel output, and the right-channel signal will be present at the right-channel output. Because switching is used in the time multiplex decoding process, unwanted transient signals are produced, which appear at the output of each channel.

Fig. 2 shows a block diagram of a typical time multiplex decoding system which employs a phase-locked loop to regenerate the subcarrier. The loop consists of a phase-locked comparator, low-pass filter, d.c. amplifier, 76kHz voltage-controlled oscillator (VCO) and two divide-by-two stages. The output from the VCO is frequency-divided twice to give a 19kHz signal. This signal is compared with the pilot-tone component of the composite input signal in the phase comparator. The output from the latter stage is fed back to the VCO, thus maintaining a phase-locked condition in the presence of a stereo broadcast. In the phase-locked loop, the 'locked' condition occurs when there is a 90° phase difference between the loop and input waveforms of 19kHz.

A pilot-tone presence detector multiplies the composite signal with a 19kHz signal from a divide-by-two stage preceded by a phase corrector. The term 'multiply' means here the combining of two in-phase signals to produce a d.c. voltage. For this purpose, the 19kHz signal is adjusted to the same phase as the pilot-tone by the phase corrector. The d.c. component is extracted by a low-pass filter and used to operate a Schmitt trigger, which in turn activates the stereo on/off gate and a lamp control. When the d.c. signal is not present at the Schmitt trigger, the stereo on/off gate prevents the operation of the decoding stage, and monophonic audio signals are passed to the left- and right-channel outputs.

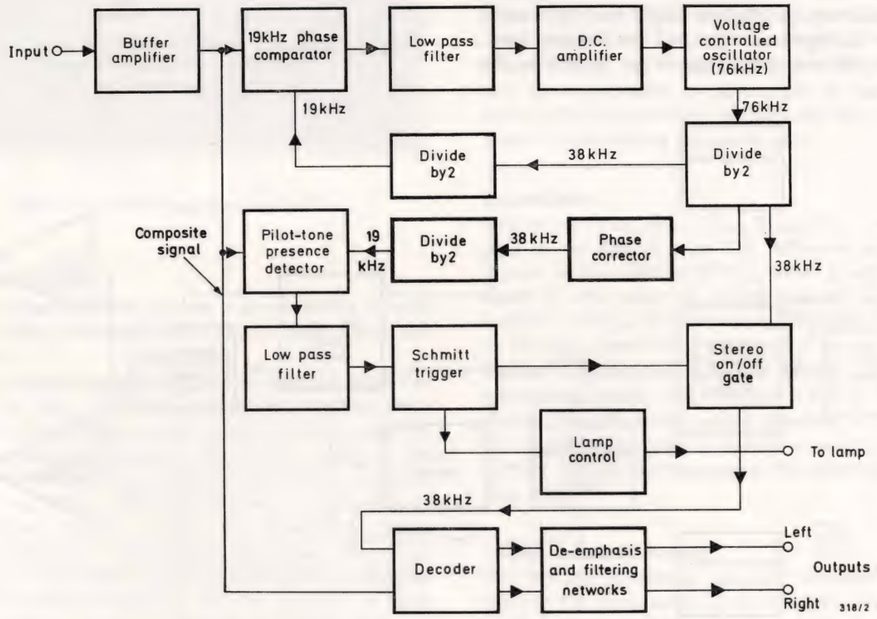

Fig. 2—Block diagram of a time multiplex decoding system which uses a phase-locked loop

FREQUENCY MULTIPLEX DECODING SYSTEM

The channel difference information is extracted in the frequency multiplex decoding system by normal techniques of amplitude demodulation. A typical frequency multiplex decoding system is shown in Fig. 3. The pilot-tone is extracted by a 19kHz resonant circuit, which can be either an active filter or (as is usually preferred) an LC tuned circuit. The 38kHz subcarrier is regenerated by doubling and filtering the 19kHz signal from the resonant circuit. The sidebands, containing the L−R (difference) information, are extracted from the composite signal through a 38kHz tuned circuit which has the response shown in Fig. 4. In this way, the difference signal sidebands are extracted and de-emphasised by a single tuned circuit. The difference signal is obtained by multiplying the extracted sidebands by the 38kHz subcarrier. Left- and right-channel output signals are obtained by combining the difference signal (L−R) with the sum signal (L+R) in a matrix circuit. The sum signal is de-emphasised after it has been extracted from the composite signal.

In the absence of a pilot-tone (monophonic condition),

the Schmitt trigger prevents the operation of the lamp control and the stereo on/off gate, which in turn disables, or 'inhibits' the demodulator. When the demodulator is in this state, monophonic audio signals are passed to the left- and right-channel outputs. The same inhibited monophonic state occurs in time multiplex decoders.

An 'inhibit' terminal is usually available on time multiplex and frequency multiplex decoders. By the application of a d.c. potential to the terminal, the Schmitt trigger in each decoding circuit switches 'off', allowing monophonic operation during stereophonic broadcasts.

RELATIVE MERITS OF THE TWO SYSTEMS

Time multiplex

The time multiplex system requires, apart from the integrated circuit, few additional components. Tuned circuits are not used and so alignment is simplified usually to the adjustment of a single potentiometer. No provision is made in a basic time multiplex circuit to compensate for audio frequency roll-off in the preceding i.f. detector of the receiver. An acceptable level of inter-channel crosstalk may therefore be very difficult to attain.

As mentioned in the description of the time multiplex decoding system, transient signals from the switched decoder stage appear at the output of each channel. To remove these unwanted signals, filtering of the outputs, in addition to the de-emphasis, is necessary.

A somewhat disturbing effect that is common to time multiplex decoders is the presence of whistling and burbling signals at the output of each channel. These signals are the result of intermodulation products of the regenerated subcarrier and the output signal of the i.f. detector preceding the decoder. To eliminate this effect, a complex filter having a sharp cut-off above 53kHz must be included between the i.f. detector output and the decoder input. Because the full composite signal is fed directly to the decoder stage, the amplitude of 19kHz and 38kHz components appearing in left- and right-channel outputs may be higher in time multiplex systems than in frequency multiplex systems.

Frequency multiplex

The frequency multiplex system is more flexible than the time multiplex system. Adjustment can be made in the frequency multiplex decoder to compensate for roll-off in the preceding i.f. detector of the receiver, ensuring minimum channel crosstalk. A dramatic reduction of the whistling and burbling signals common to time multiplex decoders is achieved in the frequency multiplex decoder by de-emphasis of the difference signal before demodulation. The controlled bandwidth of the response shown in Fig. 4 effectively removes the intermodulation products without additional complex filtering of the decoder input signal.

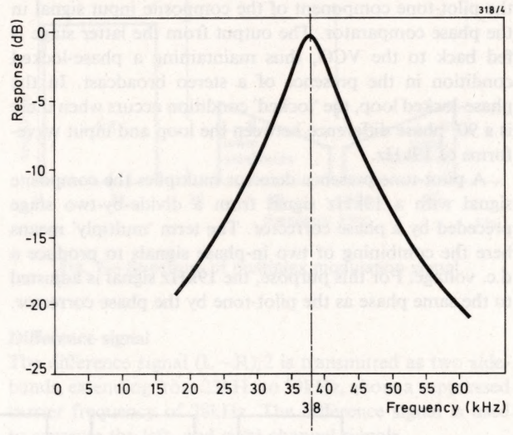

Fig. 4—Frequency response of damped tuned circuit for de-emphasis of difference signal

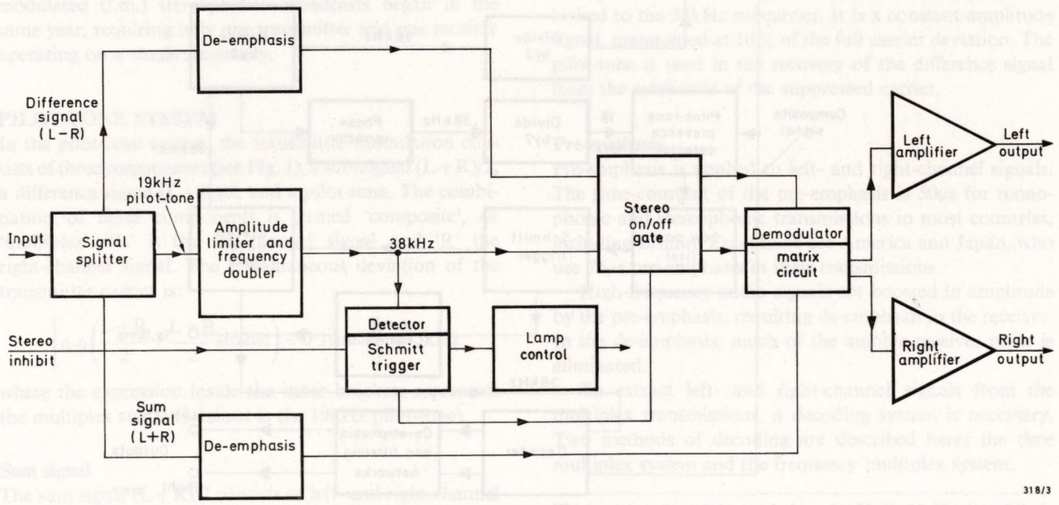

Fig. 3—Block diagram of a frequency multiplex decoding system

LP1400 STEREO DECODER MODULE

The LP1400 stereo decoder module (Fig. 5) uses the frequency multiplex system, and offers all the advantages of this system. The module is very compact, measuring only 48·5×42mm (1·9×1·65in). Two facilities for connection are available on the module; a contact strip for 'plugging-in' to a 3·81mm pitch edge connector, and vertical pins on a 5·08mm (0·2in) grid for direct or flow soldering. The modules are fully tested and aligned for optimum performance when used with an i.f. amplifier detector having a roll-off of 0·5dB at 38kHz (relative to 1kHz).

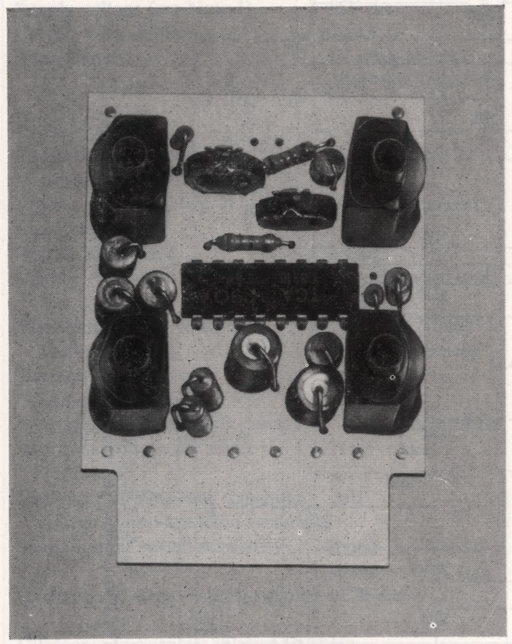

Fig. 5—LP1400 stereo decoder module

Circuit description

A circuit diagram of the module is shown in Fig. 6, with the TCA290A integrated circuit shown inside the dotted rectangle.

The composite signal is applied at point 14, via C_1 to the base of TR_1. The pilot-tone is filtered out from point 15 by L_3 and C_2. This resonant circuit also has a negative feedback action, suppressing the 19kHz signal at the collector of TR_2. The pilot-tone signal is further amplified by TR_5 and TR_7. Additional filtering is supplied by a second tuned circuit, L_4 and C_3. The phase of the 19kHz signal is adjusted by variation of L_4 inductance. Frequency doubling of the 19kHz signal is achieved by a clipping circuit comprising TR_8, TR_9, D_3, D_4, and D_5. A third tuned circuit (L_5 and C_4) extracts the 38kHz signal at point 3. This signal is used to synchronise the switching transistors TR_{11} and TR_{12}. These transistors control a demodulator (TR_{14}, TR_{15}, TR_{16}, TR_{17}, TR_{18}, and TR_{19}).

From the clipped pilot-tone signal, a d.c. component, which appears at the base of TR_{10}, is derived from D_3, D_4, and D_5. TR_{10} conducts, switching TR_{31} off. The transistors TR_{31} and TR_{32} form a Schmitt trigger. When TR_{32} conducts, TR_{33} is switched off, causing TR_{13} to conduct, activating the demodulator. Transistor TR_{34} is also switched off, causing TR_{35} to conduct and drive the stereo indicator lamp from point 11.

To prevent fluctuations in stereo operation, the frequency of 19kHz and its multiples are removed at point 12 by C_5.

Stereo inhibit

If $> 1{\cdot}3$V d.c. is applied to point 13, operation of TR_{30}, TR_{29}, TR_{28}, and TR_6 prevents TR_{32} from conducting, resulting in TR_{33} and TR_{34} being switched off. Thus stereo operation is inhibited, the demodulator is de-activated and the stereo indicator lamp is extinquished.

Difference signal

At the first stage of the module, the 19kHz signal is suppressed at the collector of TR_2, leaving only the sum (L+R) and difference (L−R) sideband signal. Transistors TR_3 and TR_4 amplify the difference signal, which is extracted by L_1, L_2, and C_6. This tuned circuit, which is damped by R_1, gives the response shown in Fig. 4. The difference signal is de-emphasised by the slope of this response before being applied, at the base of TR_{19}, to the decoding circuit.

Sum signal

Before the sum signal is applied, at point 6, to the demodulator, it is adjusted for magnitude by R_2 and de-emphasis by R_5. Roll-off in a preceding i.f. detector may be compensated by adjustment of these potentiometers. The compensation is adjustable from 0 to 2·5dB, with a corresponding change in gain.

Demodulator

Transistors TR_{14}, TR_{15}, TR_{16}, TR_{17}, TR_{18}, and TR_{19} are used in the demodulator. The difference signal (L−R) appears at the collector of TR_{21}, where it adds to the sum signal (L+R) giving the left-channel (L) signal. At the collector of TR_{22}, the difference signal −(L−R) also adds to the sum signal to give the right-channel (R) signal. Further amplification is applied by TR_{26} and TR_{27} to left-channel signals, and TR_{24} and TR_{25} to right-channel signals. The left-channel output is present at point 10 and the right-channel output is present at point 9. Capacitors C_9 and C_{10} aid the suppression of ultrasonic signals at each output.

Voltage stabilizing network

The voltage stabilizing network comprises transistors TR_{36} to TR_{40} and diodes D_7 to D_{15}. This network ensures stable operation of the module over the supply voltage range (8 to 18V d.c.).

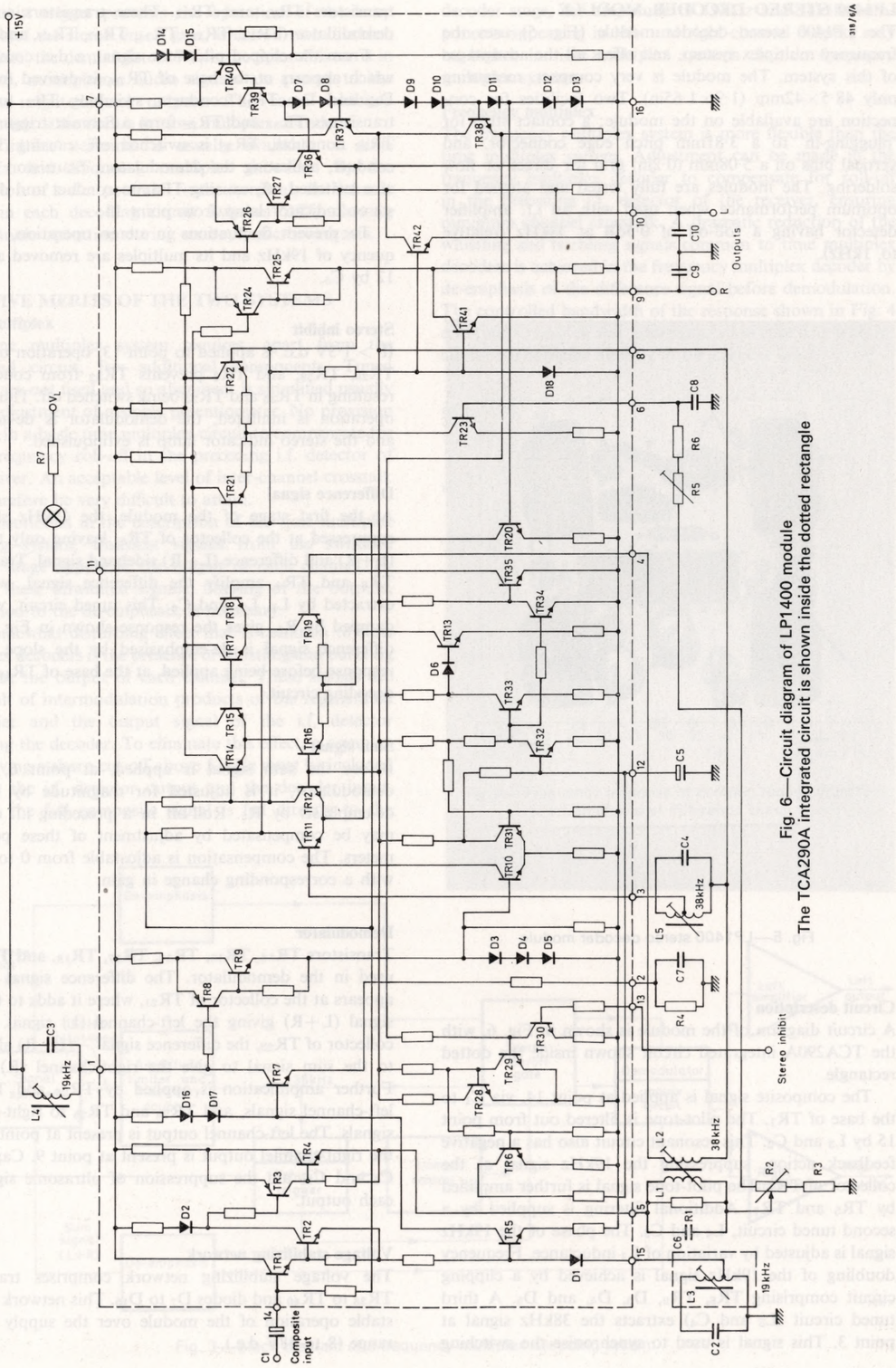

Fig. 6—Circuit diagram of LP1400 module
The TCA290A integrated circuit is shown inside the dotted rectangle

LP1400 PERFORMANCE

Typical performance figures, based on laboratory measurements of 30 modules from recent production, are listed below. Published data for the LP1400 Stereo Decoder Module should be consulted for full details of overall performance, absolute ratings and test conditions.

LP1400 Performance Data

Test conditions	
Supply voltage (see Note 1)	15V d.c.
Current consumption	20mA
Input signal	1V peak-to-peak, pilot-tone 35mV rms
Performance	
Channel separation (crosstalk) modulation 1kHz (see Fig. 7)	41dB approx.
Voltage gain (see Note 1)	10dB per channel
Input impedance	150kΩ
Output impedance	5·6kΩ
Channel balance	⩽ 1dB (mono and stereo)
Maximum output voltage (before clipping)	2·8V rms (stereo) 2·2V rms (mono)
Harmonic distortion (modulation 1kHz)	0·12%
Frequency response (3dB points)	< 20Hz to 15·8kHz
Pilot-tone voltage for stereo operation	11mV rms
Hysteresis of pilot-tone threshold voltage (mono-to-stereo switching)	1dB
Stereo inhibit switch sensitivity	mono > 1·3V d.c. stereo < 0·8V d.c.
Hysteresis of stereo inhibit voltage	0·3V d.c.
Ultrasonic frequencies relative to 1kHz	
19kHz	−42·5dB
38kHz	−48·5dB
75kHz	−18dB
77kHz	−18dB
Signal-to-noise ratio	69dB relative to 1V rms output

Note 1—low voltage operation

For operation at supply voltages between 10 and 13V d.c., resistors of 10kΩ are required between each output and earth to prevent saturation of the output transistors. When the module is operated at supply voltages between 8 and 10V d.c., the resistors are changed to 3·3kΩ. With the 10kΩ resistors in circuit at 10V supply, the module gain is reduced to approximately 6·5dB. With the 3·3kΩ resistors in circuit at 8V supply, the module gain is reduced to approximately 2dB.

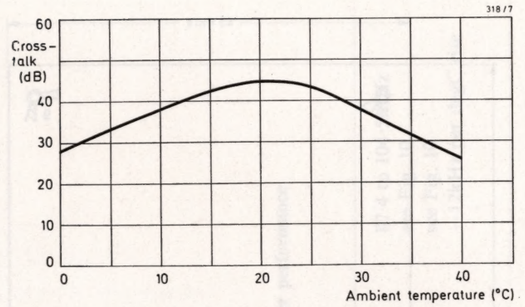

Fig. 7—Typical LP1400 crosstalk versus temperature

APPLICATIONS OF THE LP1400 MODULE

The LP1400 module is intended for use in f.m. stereo radio and tuner-amplifier equipment. Because of its compactness, the module will occupy only a small space in the equipment. The dimensions given in Fig. 8 will serve as a guide to the positioning and mounting of the module.

The circuit of an f.m. tuner which utilizes the LP1400 decoder is shown in Fig. 9. An LP1186 voltage-controlled tuner module and an LP1185 i.f. amplifier and detector module are used in the radio section. The output from the detector is decoded by the LP1400 module.

A 22μF capacitor (C_4) is connected between the output of the LP1185 and the input of the LP1400 and the latter input is shunted with a 3·9kΩ resistor (R_{12}). Together, C_4 and R_{12} form a potential divider with the output resistance of the LP1185, attenuating the amplitude of the pilot-tone before it is applied to the input of the LP1400.

To prevent oscillator drift, the tuning voltage is stabilized by TR_1, D_1, R_1, R_2, R_3, and R_4. Pre-set, push-button tuning (R_9, push-button unit 200kΩ, and R_{10}) or manual tuning (R_5, R_6, R_7, and R_8) may be selected by S_{A1}, S_{A2}.

The radio circuit supply is stabilized by D_2, R_{13}, C_3, and C_5. Overall supply stabilizing is provided by TR_2, D_3, and R_{14}. Switch S_B mutes the a.f.c., and switch S_C inhibits stereophonic operation.

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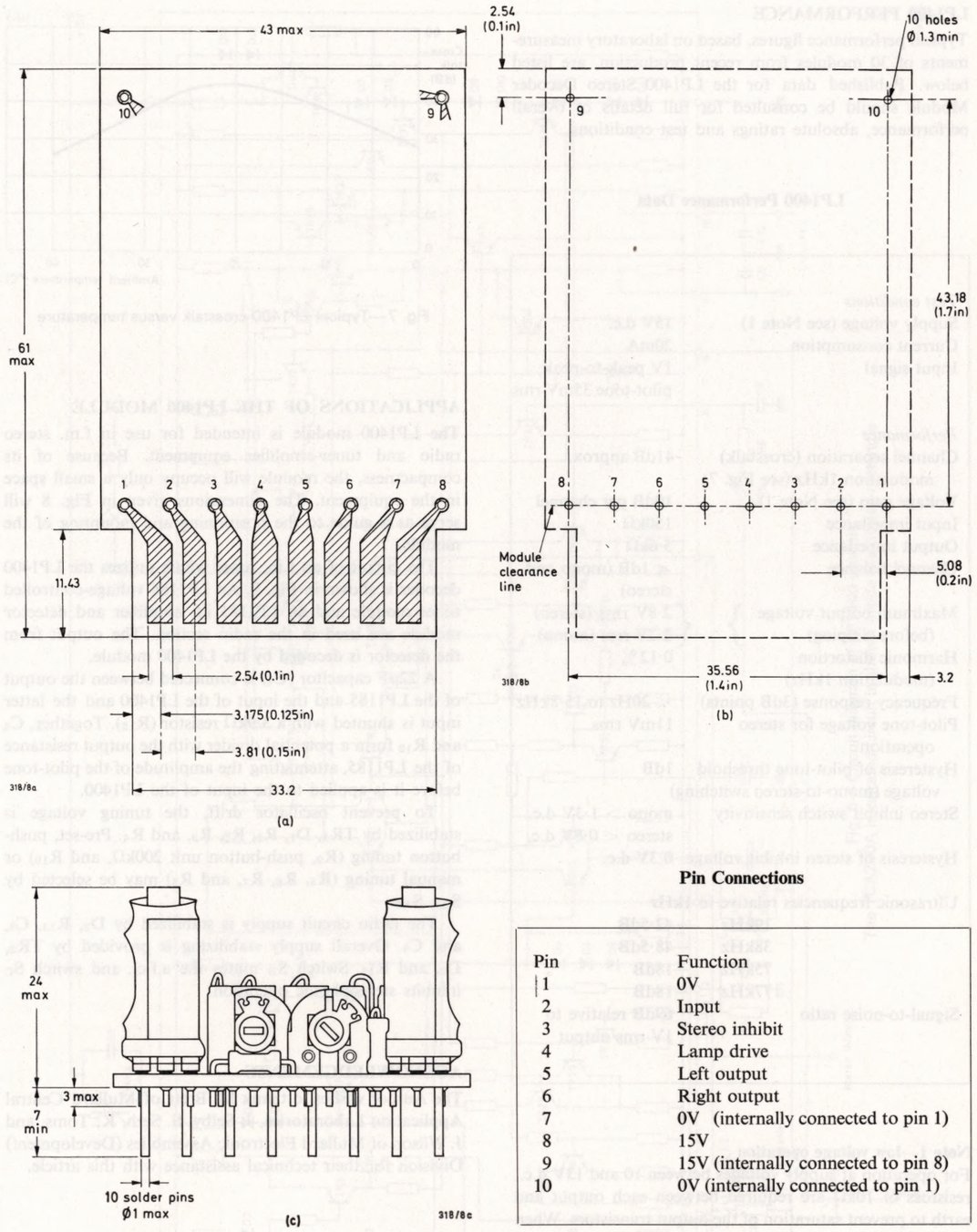
2. BBC Engineering Information Service, 'Stereophonic Broadcasting', Information Sheet 1604(4), June 1970.



Pin Connections

Pin	Function
1	0V
2	Input
3	Stereo inhibit
4	Lamp drive
5	Left output
6	Right output
7	0V (internally connected to pin 1)
8	15V
9	15V (internally connected to pin 8)
10	0V (internally connected to pin 1)

Fig. 8—Overall dimensions of LP1400 module:
(a) dimensions of board including connection pads
(b) piercing diagram (view from component side of board) (c) overall height of module, and diameter of pins
All unspecified dimensions in mm

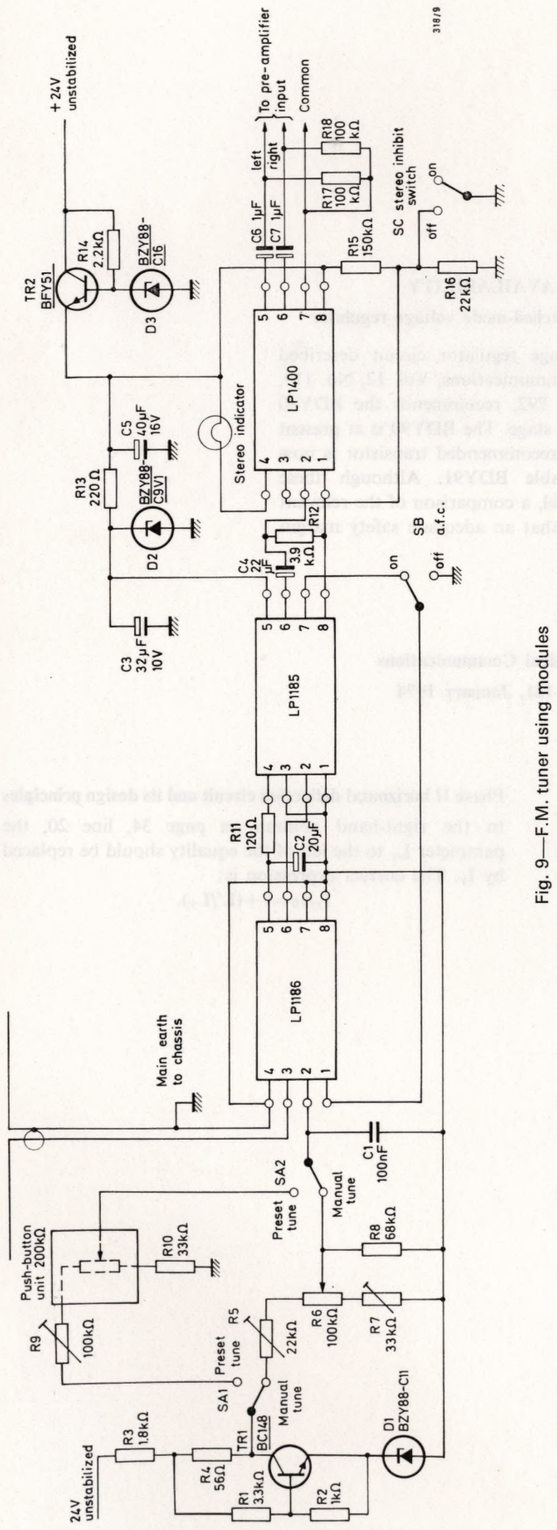


Fig. 9—F.M. tuner using modules

F.M. tuner performance

Tuning range	87·4 to 104·5MHz
Sensitivity	see Fig. 10
Signal-to-noise ratio	see Fig. 10
Frequency stability without a.f.c.	—12kHz per degC rise

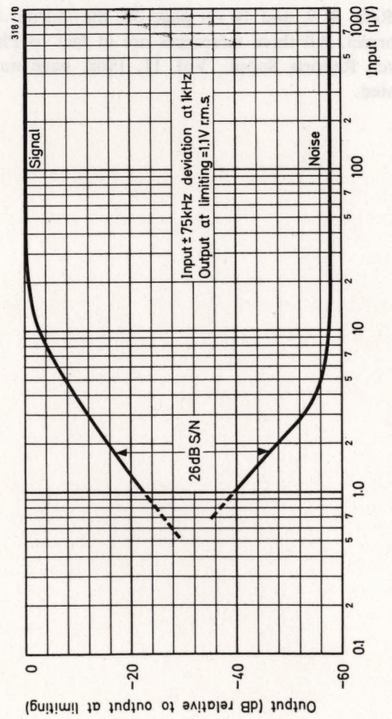


Fig. 10—Sensitivity and signal-to-noise ratio of the f.m. tuner

DEVICE AVAILABILITY

Variable 35V 10A switched-mode voltage regulator

The switched-mode voltage regulator circuit described in Mullard Technical Communications, Vol. 12, No. 119, July 1973, pages 279 to 292, recommends the BDY90 as suitable for the output stage. The BDY90 is at present in short supply, and the recommended transistor is now the more readily available BDY91. Although these transistors are not identical, a comparison of the relevant characteristics will show that an adequate safety margin still exists in this circuit.

Mullard Technical Communications
Vol. 13, No. 121, January 1974

Deflection system design for 110° shadowmask tubes

In Refs. 8, 9, and 10 on page 30, the journal quoted is incorrect. All three references are in fact to Philips Research Reports Suppl., Vol. 11, 1968, page numbers as printed.

Phase II horizontal deflection circuit and its design principles

In the right-hand column on page 34, line 20, the parameter L_y to the left of the equality should be replaced by I_y. The correct expression is:

$$I_y/I_0 = 1 + (L'/L_y).$$